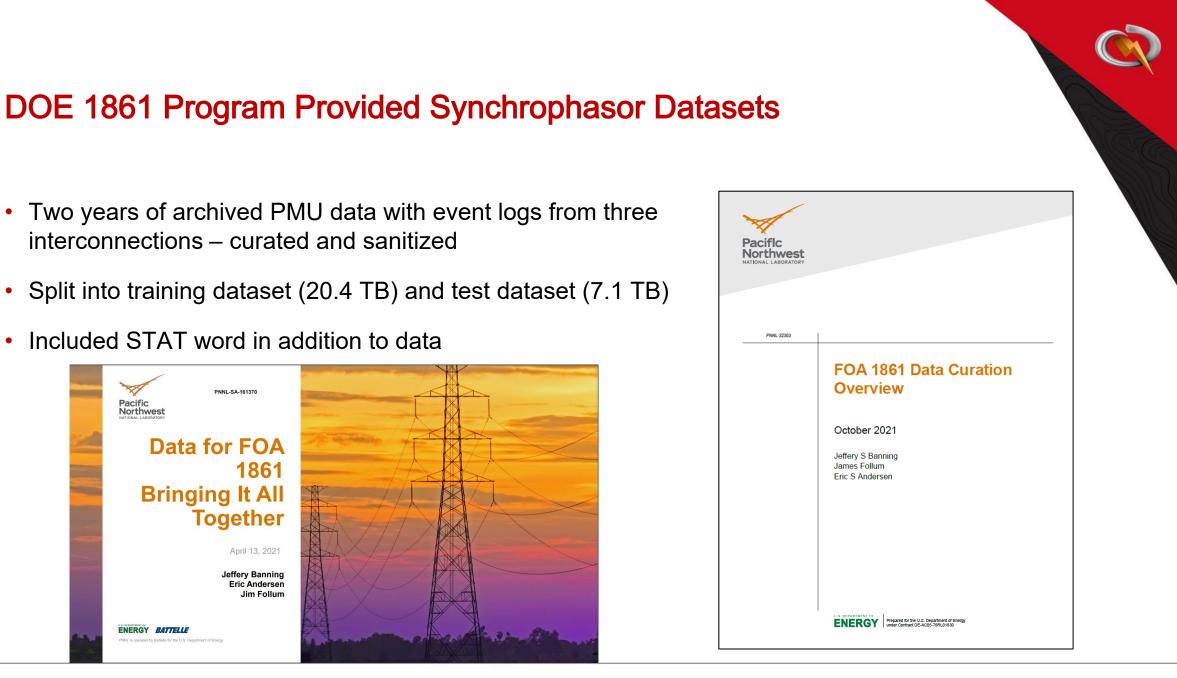


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Synchrophasor System Data Quality – Can We Do Better?

Yi Hu, Zheyuan Cheng

NASPI Work Group Meeting, April 2023, Tempe, AZ

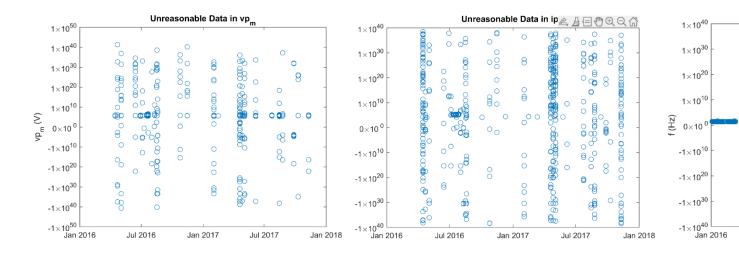


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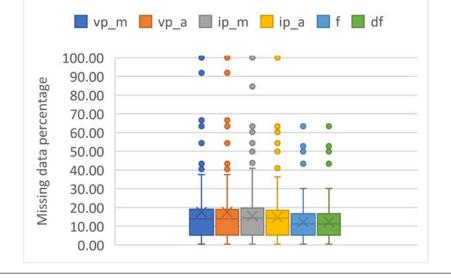
Key Observations from Datasets Provided by DOE in 1861 Program



Common issues seeing among 188 PMUs

- Missing data most missing 5%20% and some even more
- Unreasonable values out of normal range

Z. Cheng, Yi Hu, Z. Obradovic, and M. Kezunovic, "Using Synchrophasor Status Word as Data Quality Indicator: What to Expect in the Field?" IEEE PES SGSMA 2022, May 2022



Unreasonable Data in f

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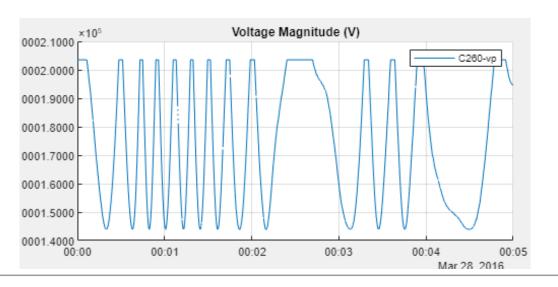
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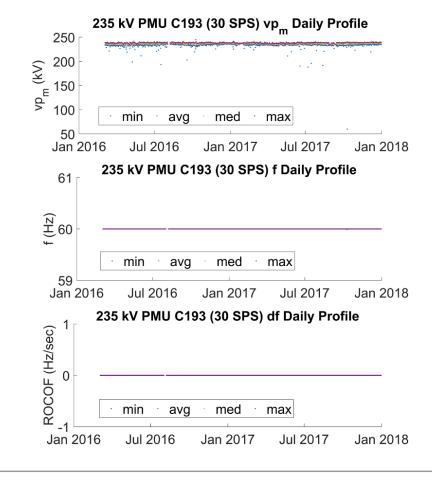


Key Observations from Datasets Provided by DOE in 1861 Program

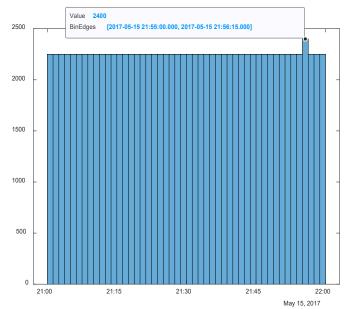
Unique issues

- One PMU has a fluctuating voltage magnitude between 145kV and 205kV
- 18 PMUs show constant 60 Hz frequency value



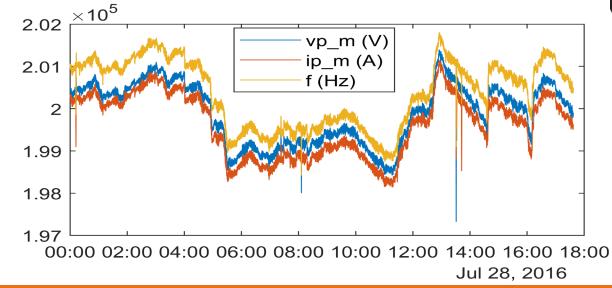


Key Observations from Datasets Provided by DOE in 1861 Program



Other issues

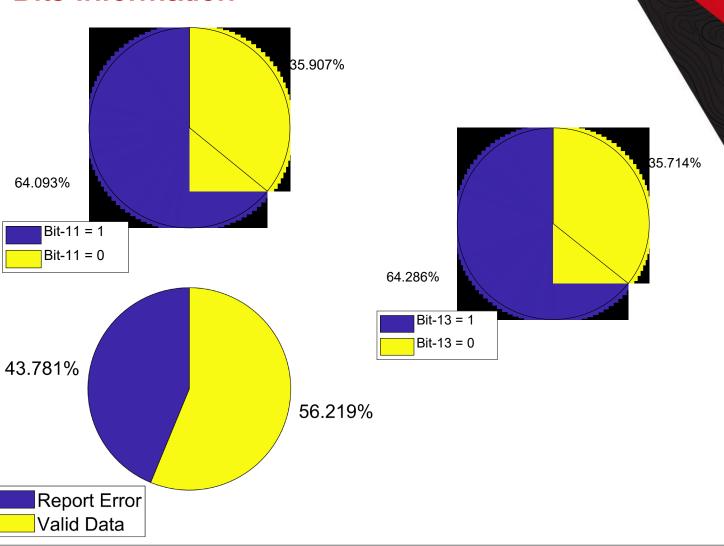
- Duplicated data
- Misplaced data
- Time tag format variations



Type-I	Type-II	Type-III
'00:00:00.00000000'	'00:00:00.00000000'	'00:00:00.00000000'
'00:00:00.033 <mark>34</mark> 0000'	'00:00:00.033000000'	'00:00:00.033000000'
'00:00:00.066 <mark>68</mark> 0000'	'00:00:00.06 <mark>7</mark> 000000'	'00:00:00.06 <mark>6</mark> 000000'
'00:00:00.10000000'	'00:00:00.10000000'	'00:00:00.10000000'
'00:00:00.133 <mark>34</mark> 0000'	'00:00:00.13 <mark>3</mark> 000000'	'00:00:00.13 <mark>2</mark> 000000'
'00:00:00.166 <mark>67</mark> 0000'	'00:00:00.16 <mark>7</mark> 000000'	'00:00:00.16 <mark>5</mark> 000000'
'00:00:00.2000 <mark>1</mark> 0000'	'00:00:00.20000000'	'00:00:00.20000000'
10 PMUs	80 PMUs	98 PMUs

Unable to Use/Trust The STAT Bits Information

- No standard version number (2005 or 2011) in the dataset
- Inconsistent bit setting
 - Trigger bit 11 vs. Trigger Condition bits 03-00
 - Sync bit 13 vs. Unlocked Time bits 05 04 and Time Quality bits 08-06 (2011)
 - Data Quality bits 1514 vs. Sync bit 13
- Poor correlation of the data quality between observed and Data Quality bits 1514 indicated



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What Could We Do to Improve Synchrophasor System Data Quality?

Standards

- Specify clear STAT bits definitions and the associated conditions to set and reset nothing should be subject to implementer's interpretation
- Add missing information e.g., ensure version number is available both in real-time data and in archived data
- There are many more areas welldone standardization could help
- Certification testing
 - An effective way to ensure all products will function and perform the same according to the same standard

- Adopt system designs that enable higher data availability
 - Enable fast data missing issue identification and location
 - Avoid system designs that may cause data quality issues
 - Prone to single-point of failure
 - Data may be dropped by certain intermediate system component
 - Impacted by communication protocol choices

Enable Fast Data Loss Detection and Remediation

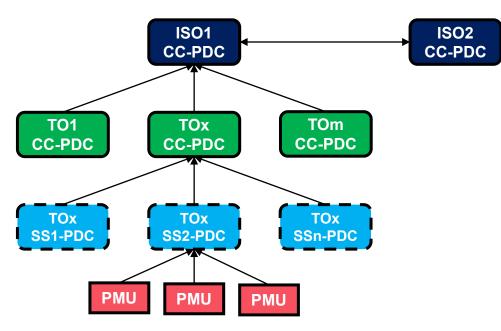
Current best practices

- Monitor the data availability at the data receiving or consumption point continuously
- Generate alarms or notifications when excessive data loss is detected (i.e., triggered by targeted availability threshold)
- Trace the data flow path until the source of the data loss is determined
- Remedy the situation to prevent future data losses
- The issues
 - Data losses below the threshold may not get much attention, let alone to fix them – some of such losses could evolve to cause major losses
 - Tracing the data flow path to find the data loss source is a time consuming task when involve multiple entities
 - Difficult to trace non-repeatable data loss incidents

- A synchrophasor system could be its own automated data loss monitoring system
 - Each intermediate data transferring component (IDTC such as PDCs, Gateways, etc. that receive and resend the data) knows its own data loss situation in detail
 - Save such info at each IDTC will enable source of the data losses to be determined much faster
 - Send such info to downstream IDTCs or enduse point
 would enable automated data loss source determination
- The result
 - Faster detection and remediation → Short data loss duration → Higher data availability
- What can be done?
 - A NASPI guide line?
 - An IEEE standard?

Design Synchrophasor System for High Data Availability

- CC-PDC Control Center PDC
- SSn-PDC Substation n PDC



<u>Typical System Design</u>

- Include built-in redundancy
 - System level make everything redundant, or
 - Only the ones that have more impact on the data losses
- Aware intermediate PDC could drop data that are arrived too late
 - Wait or not wait?
- Choose data transfer protocol appropriately
 - TCP or UDP?
 - Unicast or multicast?

Conclusions

- There are still rooms for further improvement in synchrophasor systems data quality
- It will take a concerted effort by all stakeholders to properly address all known and emerging issues that impact the data quality
- While great progresses have been made, the data availability of synchrophasor systems could be further improved
- System design choices could have a direct impact on a synchrophasor system's data availability

Thank You!



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