Impact of Synchrophasor Data Quality on Low-Frequency Oscillation Control

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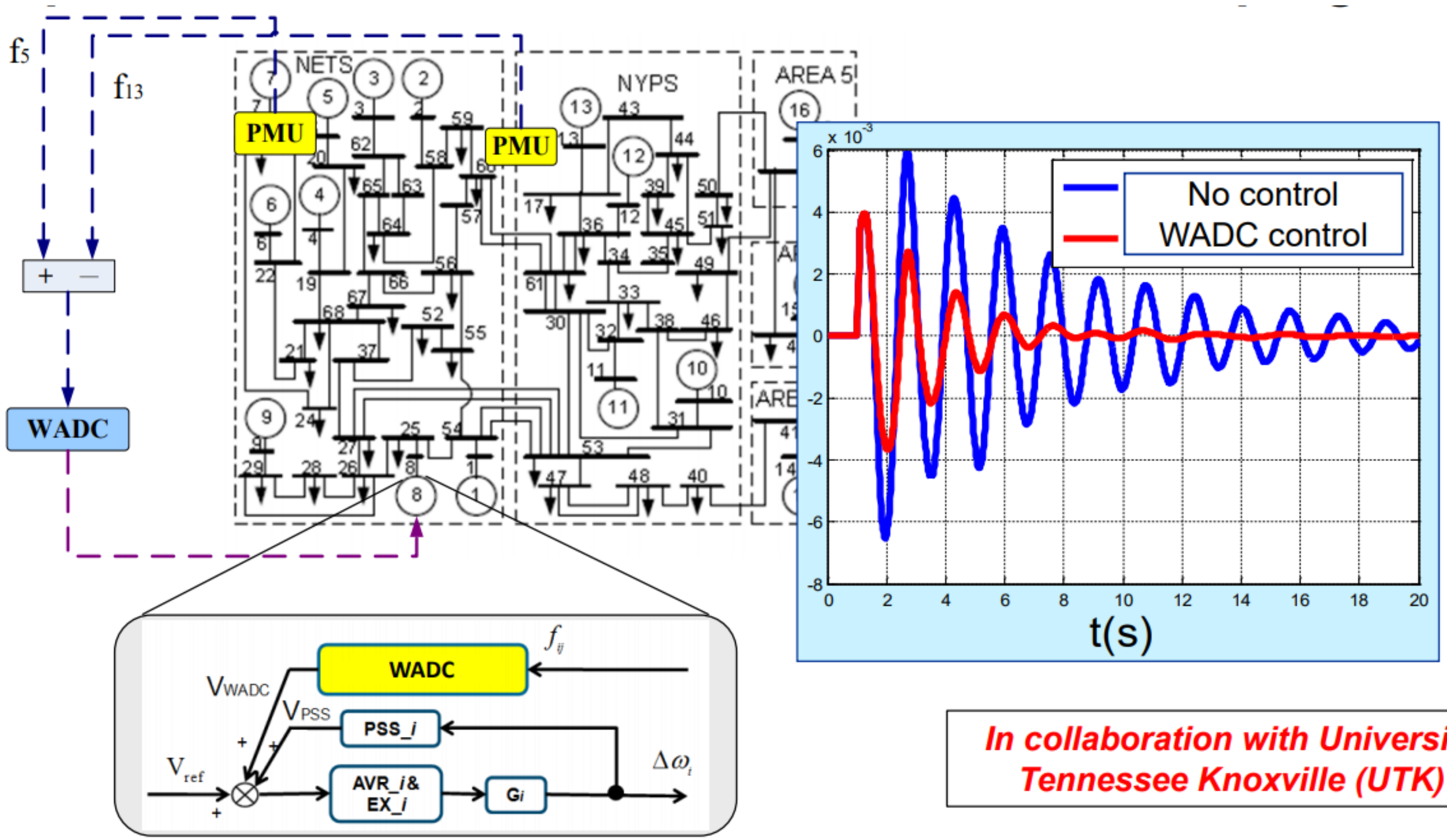
Synchrophasor-Based Wide-Area Oscillation Damping Control

- Application of synchrophasor technology in closed-loop wide area control
- Improve damping of target inter-area/intra-area oscillation modes
- Case study on EPRI members' power grid models by computer simulations and hardware-in-the-loop testing:
  - NY State
  - Continental Europe
  - Saudi Arabia
  - Great Britain

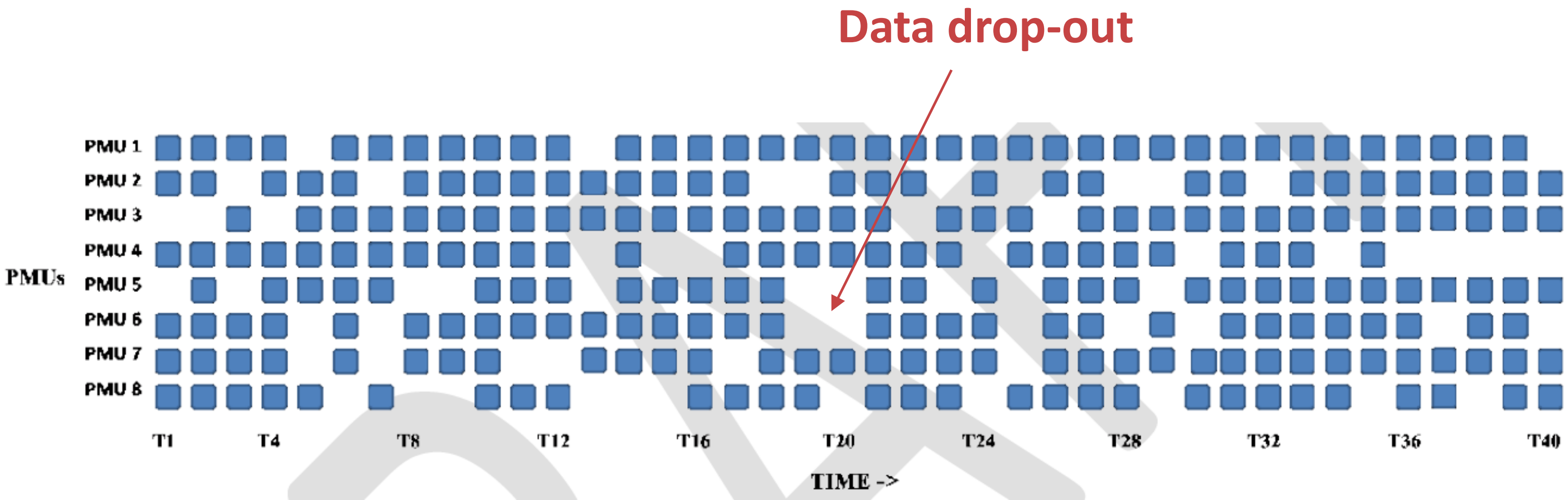


In collaboration with University Tennessee Knoxville (UTK)

The University of Tennessee Knoxville

Synchrophasor Data Quality Issues

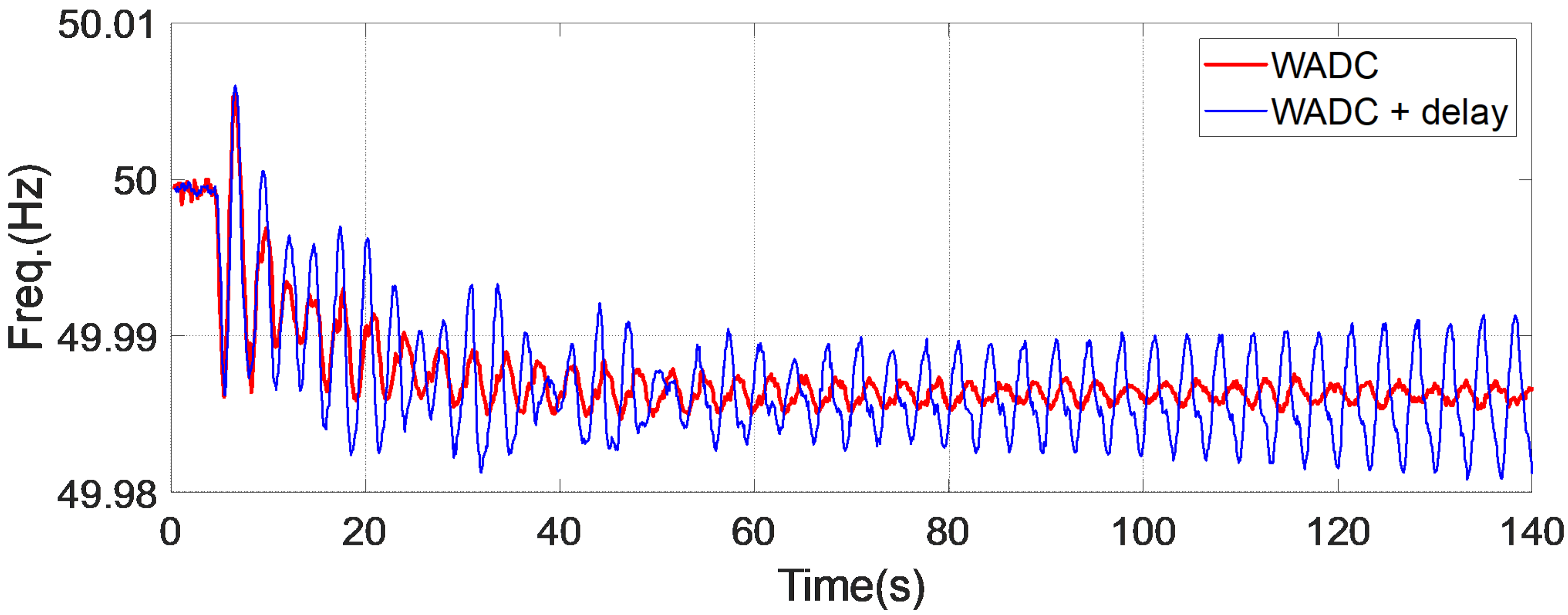
- Data quality could significantly impact any synchrophasor-based applications, especially in closed-loop wide area control
  - Bad headers
  - Bad measurement
  - Bad timestamp
  - Time delay (latency)
  - Data drop-out
  - Others
- Constant/random delay and occasional/consecutive data drop are investigated in this study.



Source: NASPI PMU Applications Requirements Task Force, Synchrophasor Data Quality Attributes and a Methodology for Examining Data Quality Impacts upon Synchrophasor Applications, March 2016

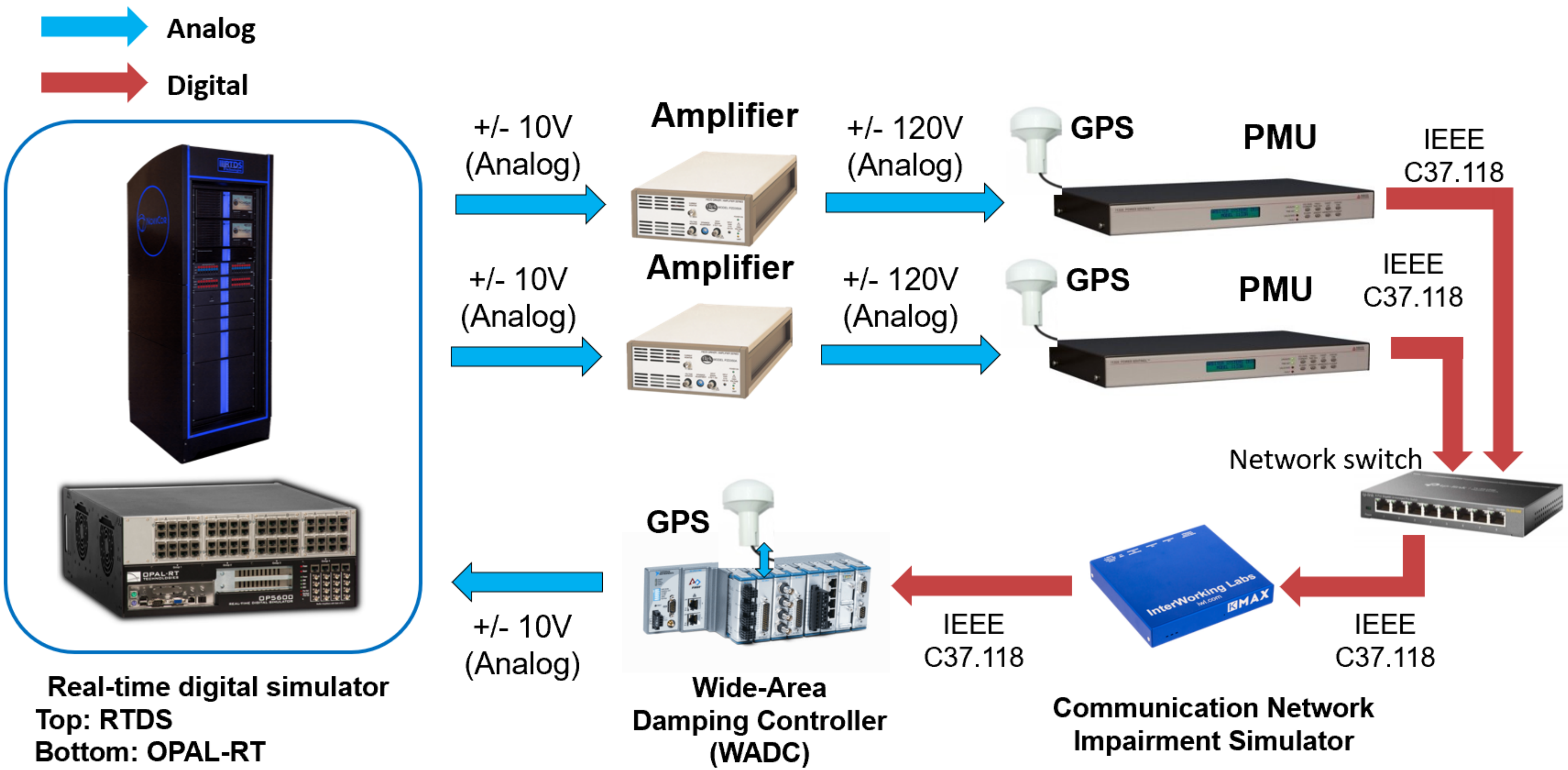
Impact of Time Delay on WADC

- Typically time delay is not modeled in offline dynamic simulations
- Random time delay can deteriorate WADC performance



Impact of Time Delay on WADC

Controller Hardware-In-the-Loop Test Setup



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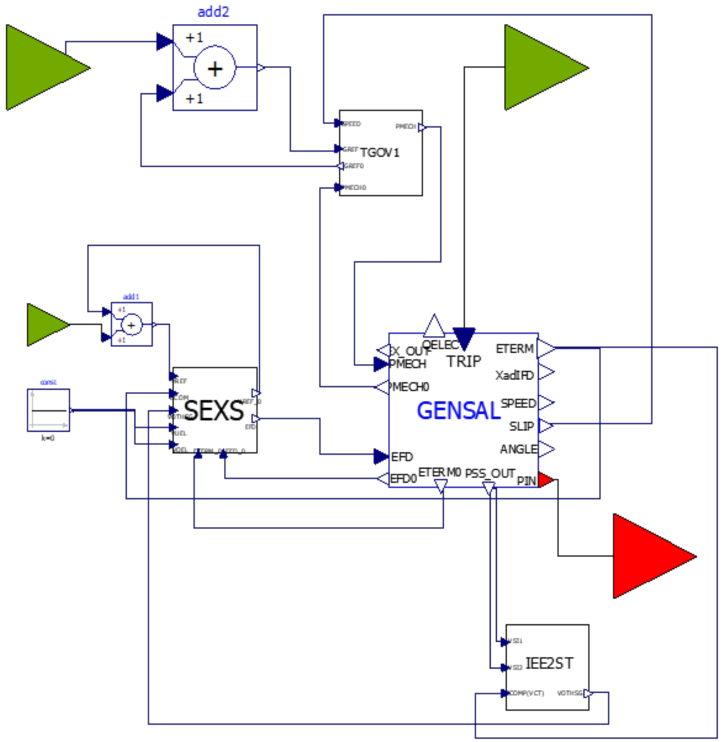
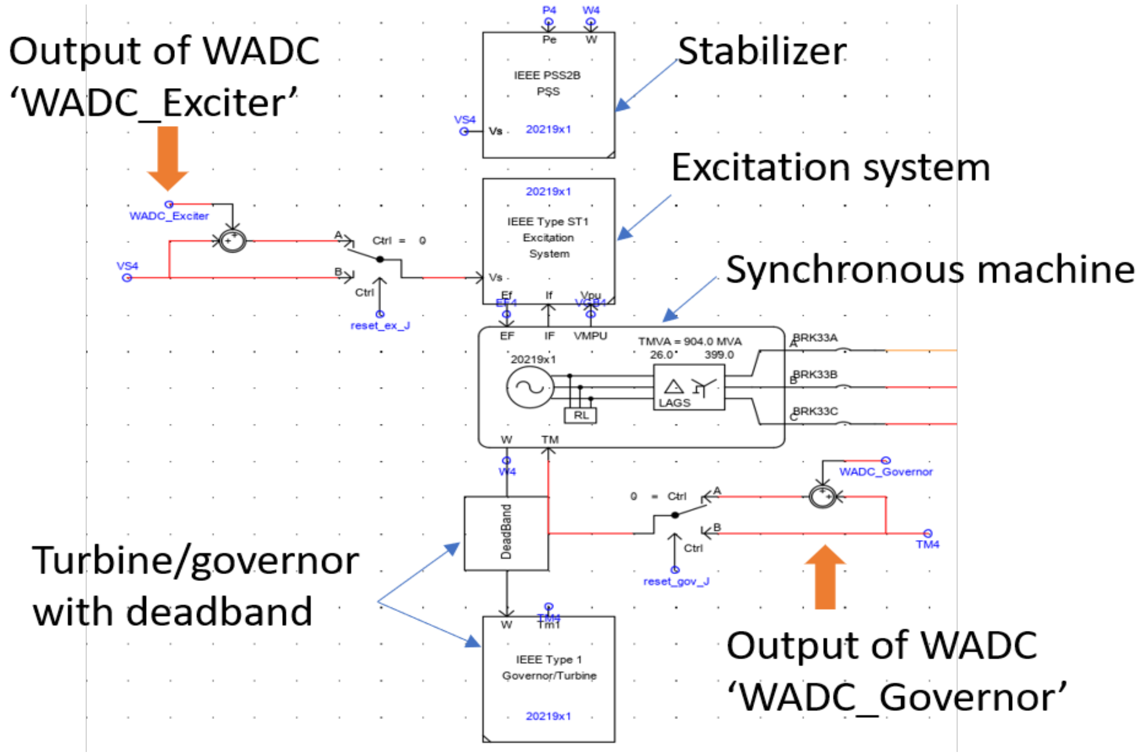
Grid Model Implementation for Real-Time Simulation

- OPAL-RT: ePHASORSIM model
- RTDS: RSCAD model



OPAL-RT ePHASORSIM model



RTDS RSCAD model

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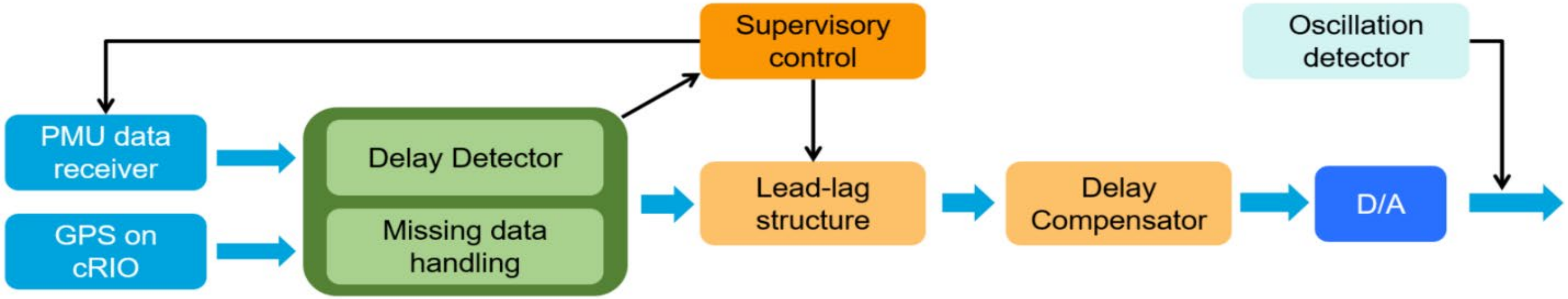
Controller Implementation on Generic Hardware Platform

		Block Name	Function
Basic Module	1	PMU data receiver	Unpack PMU data package complying with C37.118
	2	Lead-lag structure	Basic control function
	3	D/A conversion	Convert digital signal to analog signal
Advanced Module	4	GPS module	Capture absolute timestamp
	5	Delay detector	Estimate the time delay
	6	Delay compensator	Eliminate impact of time delay
	7	Missing data handling	Eliminate impact of missing data
	8	Supervisory control	Switch PMU channel, identify transfer function model (to be added), determine optimal controller parameters (to be added)
	9	Oscillation detector	Disable controller if no oscillation



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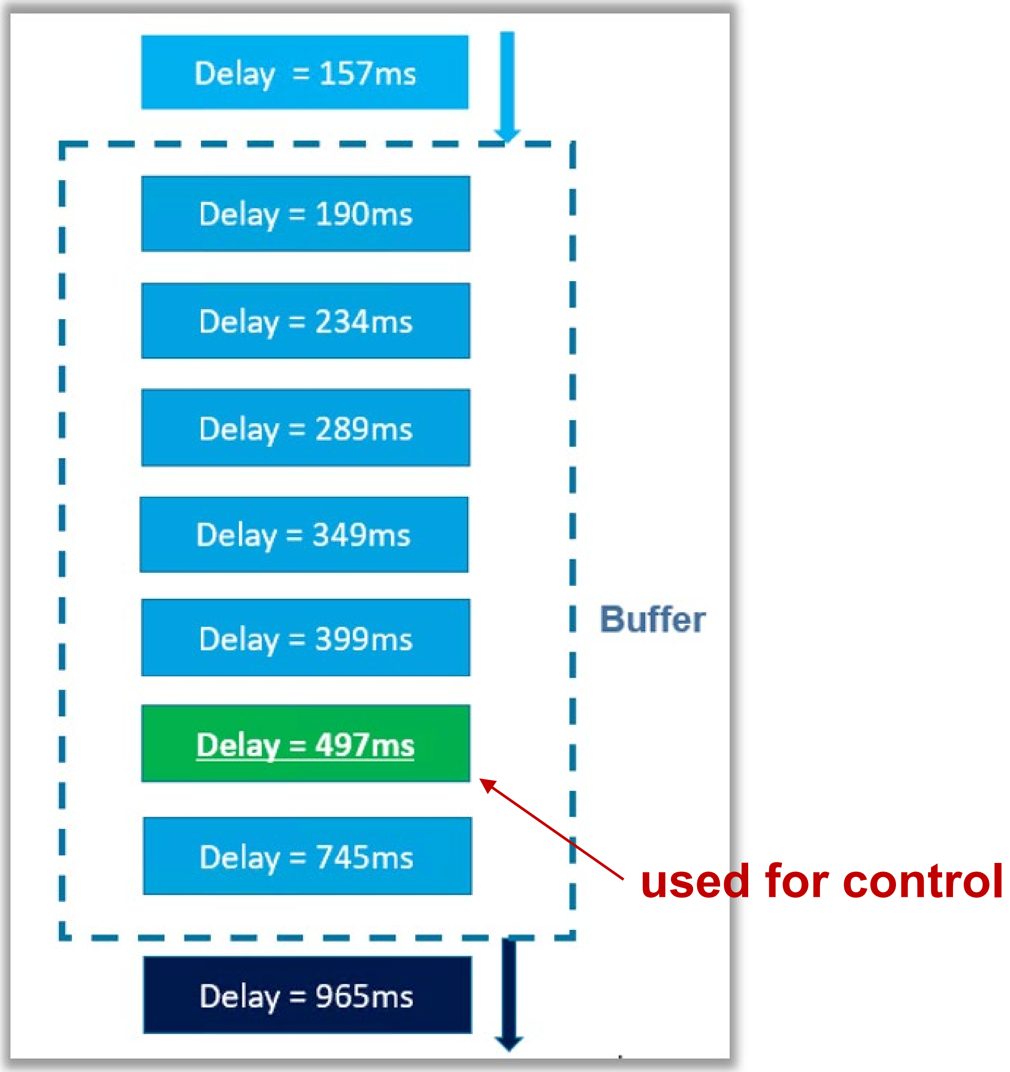
Constant/Random Delay Compensation with a Buffer

- Compare Timestamp A and B
  - Timestamp A: PMU measurements are generated
  - Timestamp B: Controller receives measurements
- Use a lead-lag structure to compensate phase shift due to time delay
- Control with buffered data, e.g., buffer size = 500 ms
  - Convert random delay to constant delay
  - PMU reporting rate: 25/30Hz, 50/60Hz
  - WADC control rate: 10Hz
  - Use the package with delay closest to 500 ms to generate control command
  - Buffer size is typically equal or smaller than the max. tolerable delay.



Control with buffered data - constant delay compensation (500ms)

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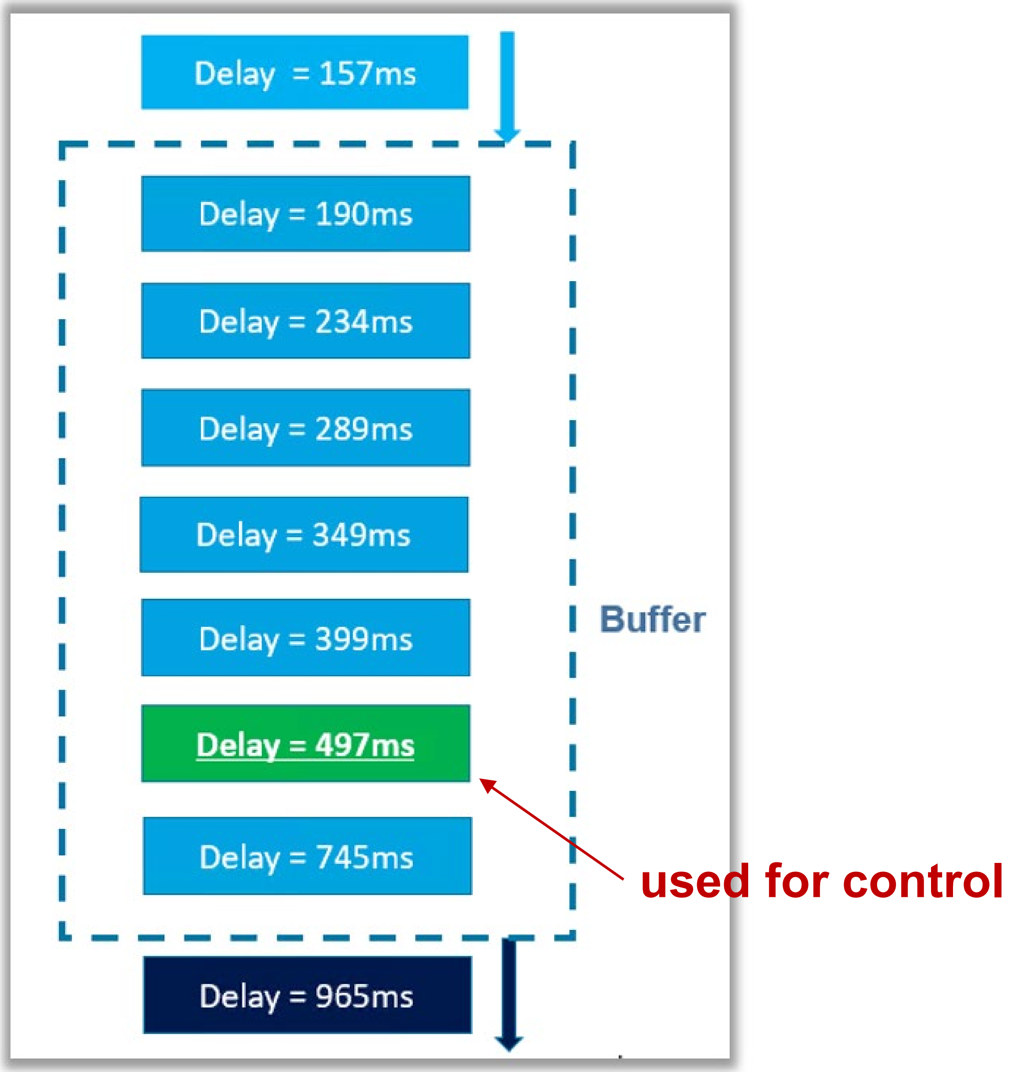
Occasional Data Drop Handling

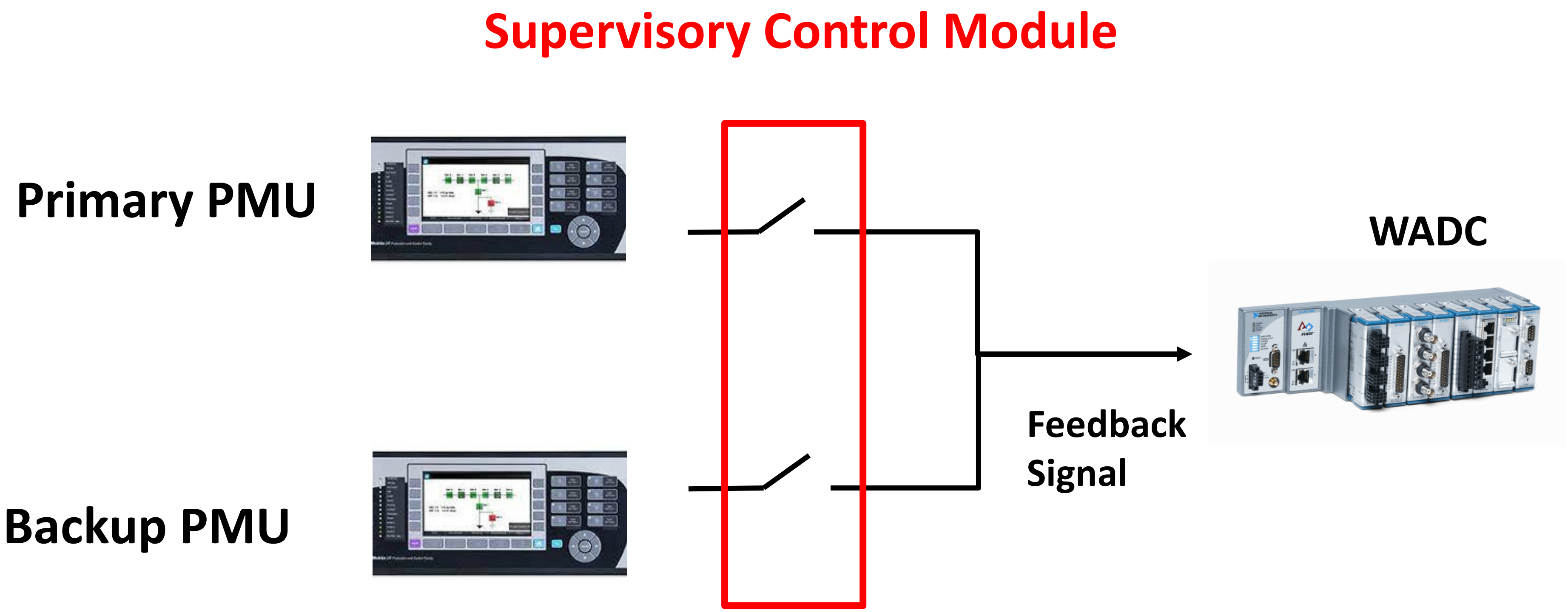
- Control with buffered data
  - PMU reporting rate (30Hz) > control rate (10Hz)
  - Multiple data points are available in the buffer for each control cycle.
  - Occasional data drop does not impact control
  - Controller can hold its previous command if no data point is available for present control cycle.
  - If delay is larger than the buffer size, treated as data drop.



Control with buffered data - constant delay compensation (500ms)

Supervisory Control to Handle Consecutive Data Drop

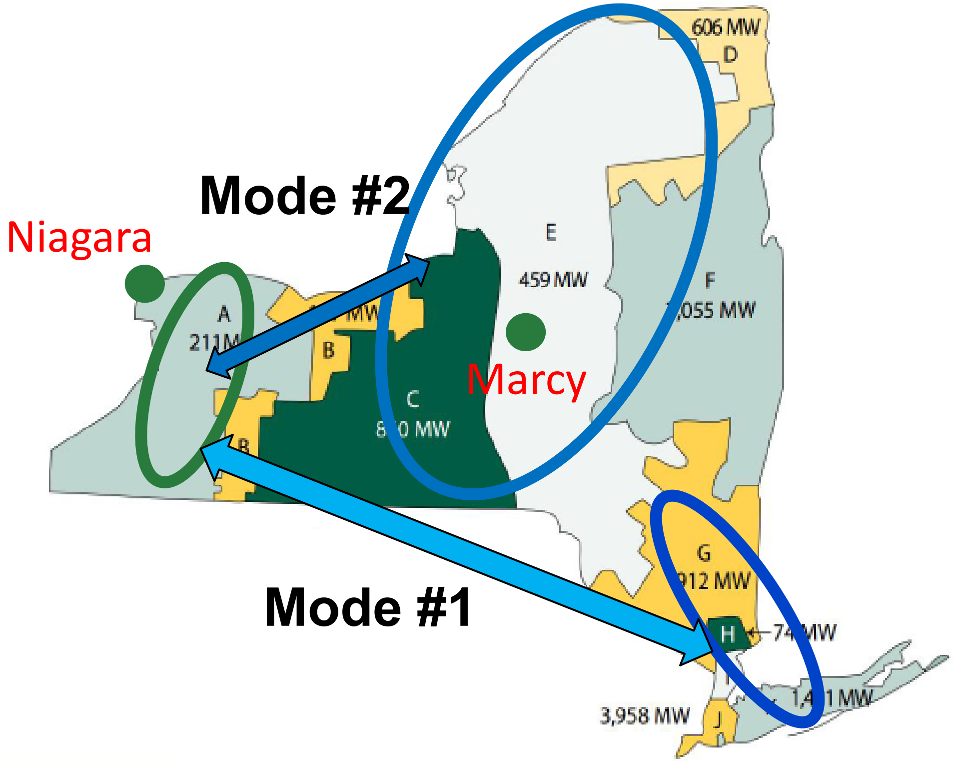
- Supervisory control:
  - Switch to backup PMU in case of long delay or loss of primary PMU
  - Switch back to primary PMU if its performance is satisfactory



Case Study Systems

- 2019 planning model: 70k-bus
- Two modes: West-North and West-South
- Input signal: Bus frequency difference A and E
- Actuator: Niagara generators

- 2k+ bus model with 2017 event replicated in simulation
- Target mode: South Italy v.s. France/Germany
- Input signal: South Italy local frequency
- Actuators: Two synchronous condensers in South Italy



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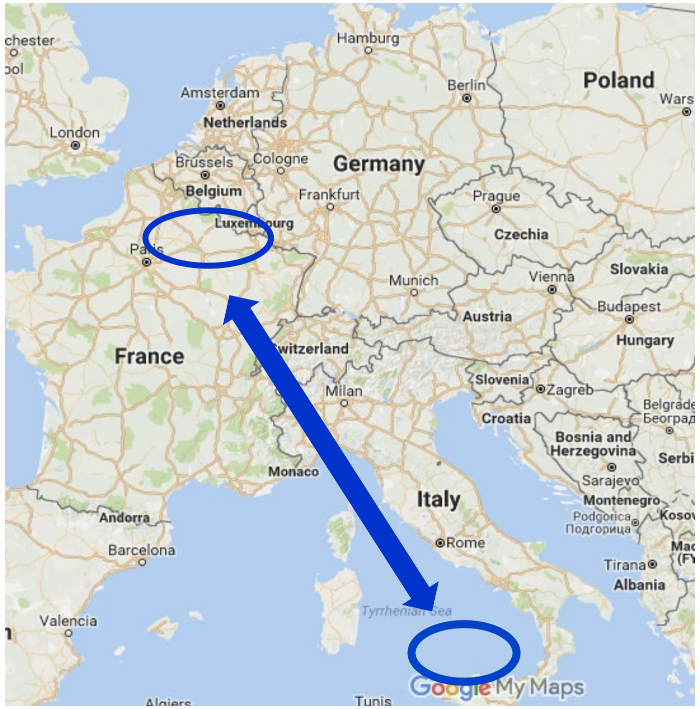
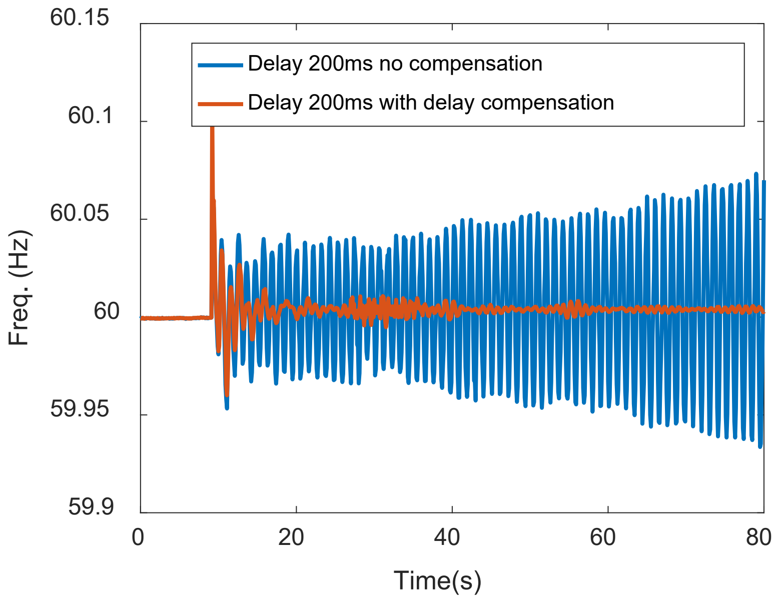
New York State Power Grid



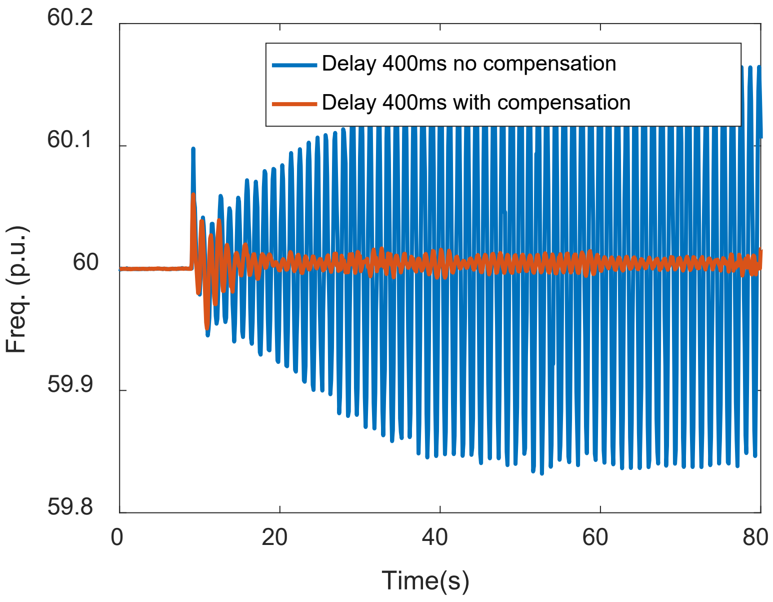
Continental Europe Power Grid

HIL Test Results: NY State Power Grid

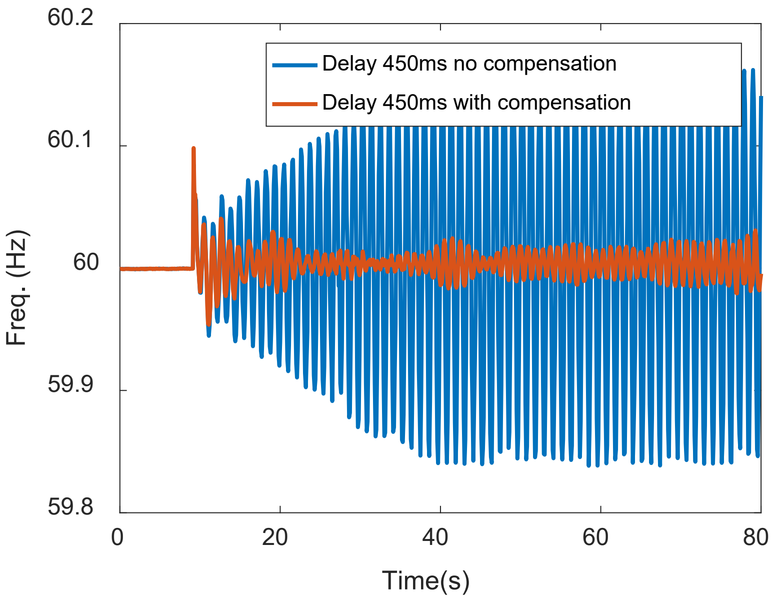
- Constant Time Delay (PMU reporting rate = 30Hz, control rate = 10Hz)
  - Intrinsic closed-loop delay: around 200ms (unstable without compensation)
  - Additional time delay is introduced by network impairment simulator
  - The maximum tolerable time delay: about **400ms**



200 ms constant delay



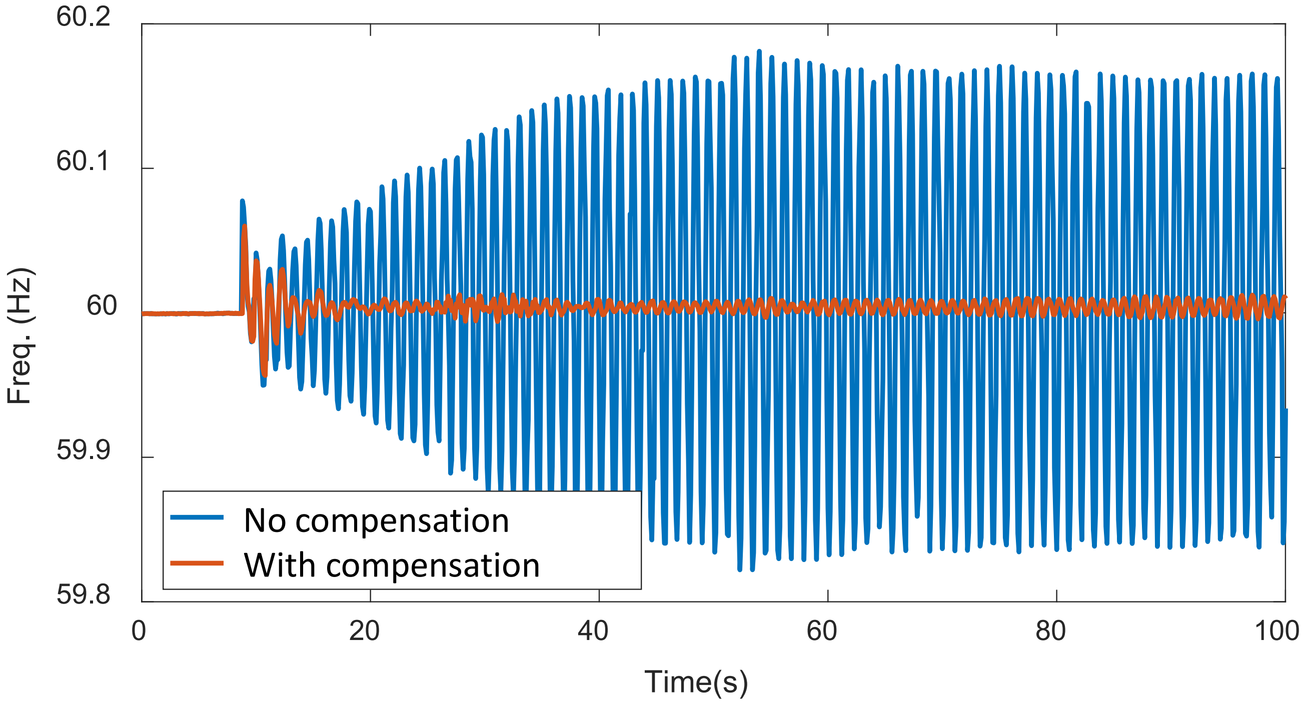
400 ms constant delay



450 ms constant delay

HIL Test Results: NY State Power Grid

- Random Time Delay (PMU reporting rate = 30Hz, control rate = 10Hz)
- Delay compensation with a buffer (butter size = 400 ms)
  - Random delay (300ms mean value + 100ms variation)
  - With the delay compensation, the system remains stable.



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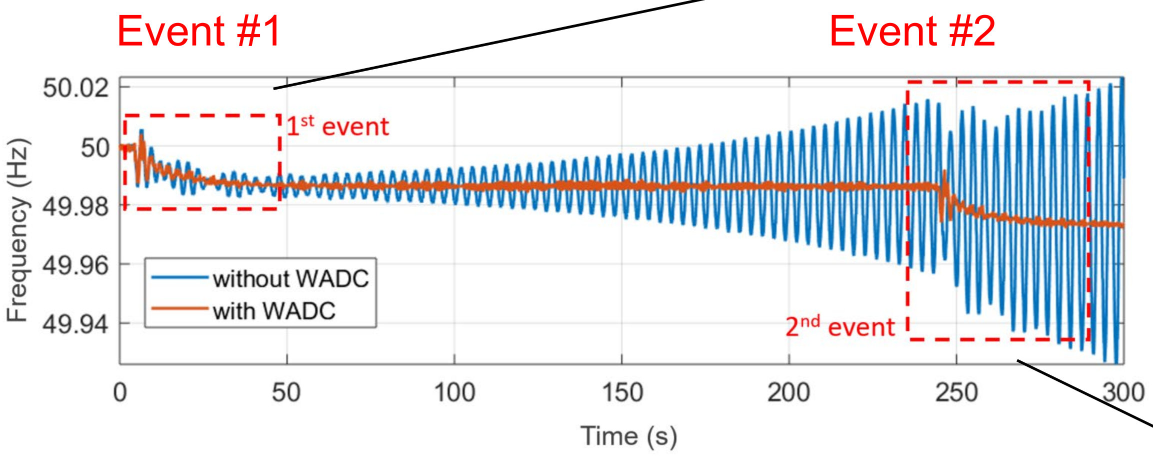
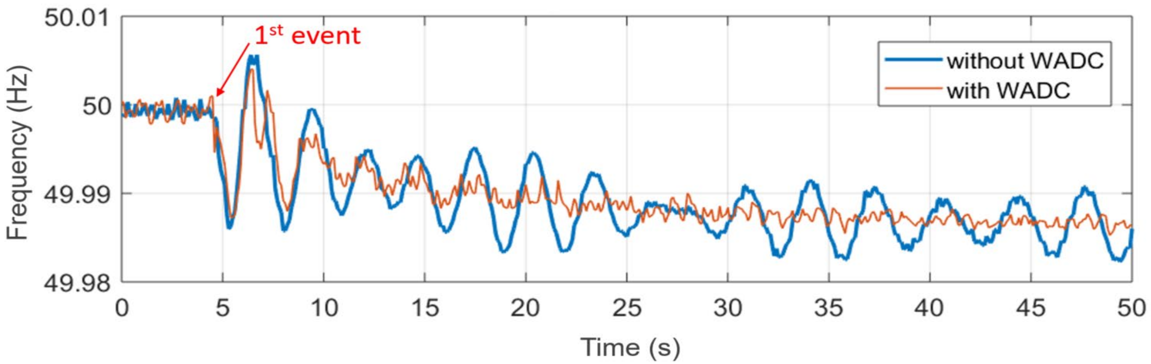
HIL Test Results: Continental Europe Power Grid

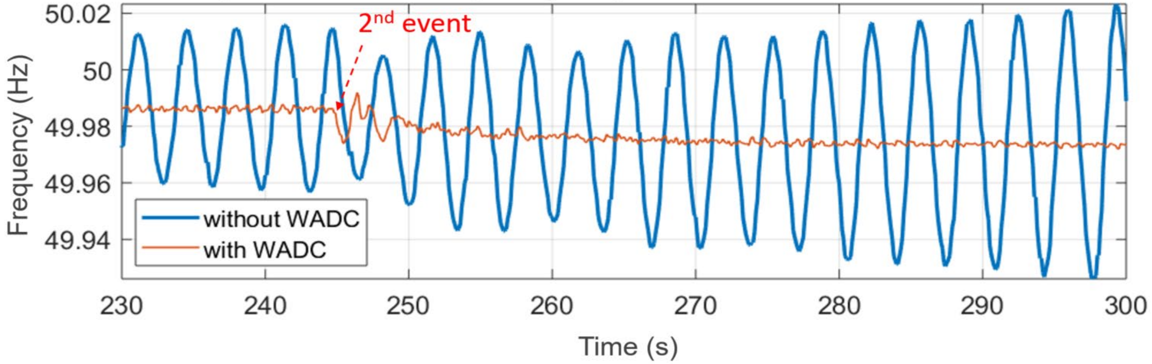
- No Time Delay + No Data Loss
  - Dec. 3, 2017 actual oscillation event: Event #1 at 5s, Event #2 at 245s
  - Actuator: two synchronous condensers in South Italy
  - Input signal: Bus frequency in South Italy



Bus frequency in South Italy



Details around the first event



Details around the second event

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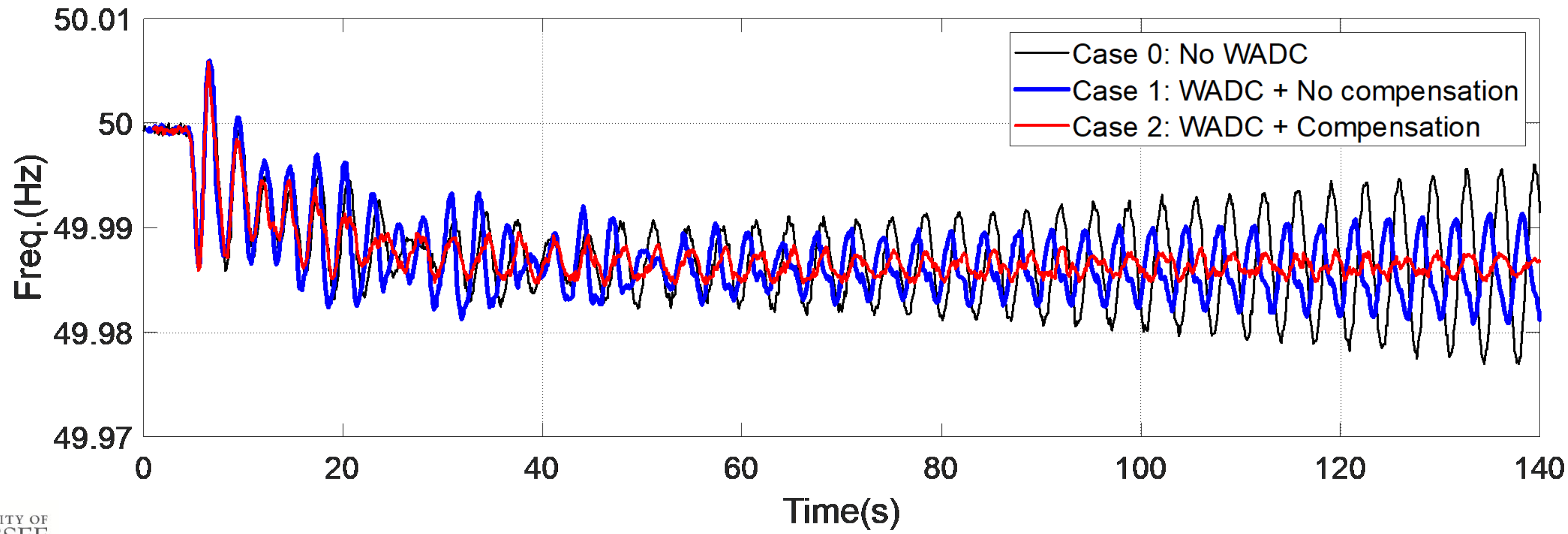
HIL Test Results: Continental Europe Power Grid

- PMU reporting rate: 25Hz; Control rate: 10Hz; Buffer size: 800 ms
- 150-950 ms random delay + 60% random data loss
  - **Case 0:** No WADC
  - **Case 1**: WADC + No compensation & Missing data handling
  - **Case 2: WADC + Compensation & Missing data handling**



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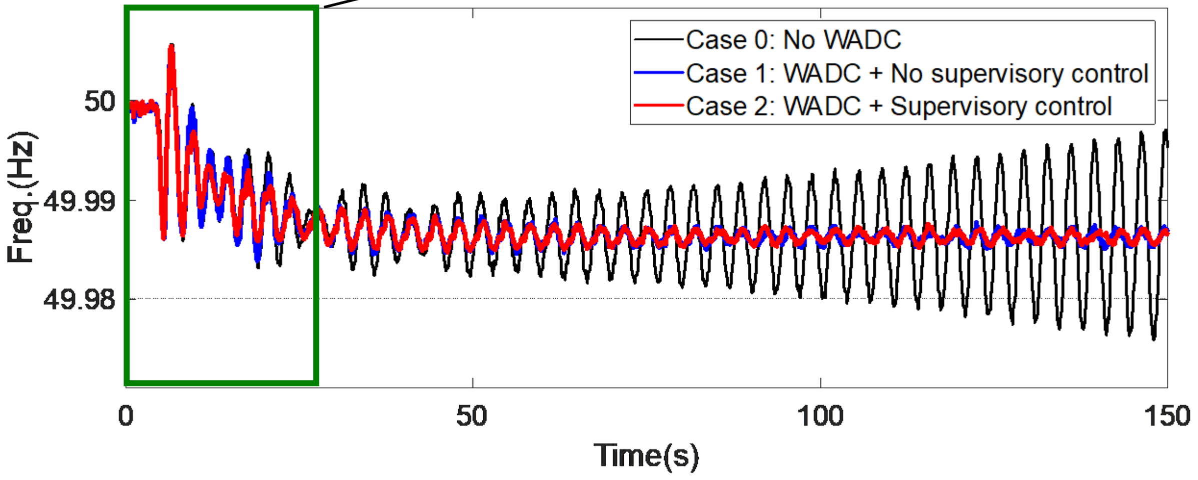
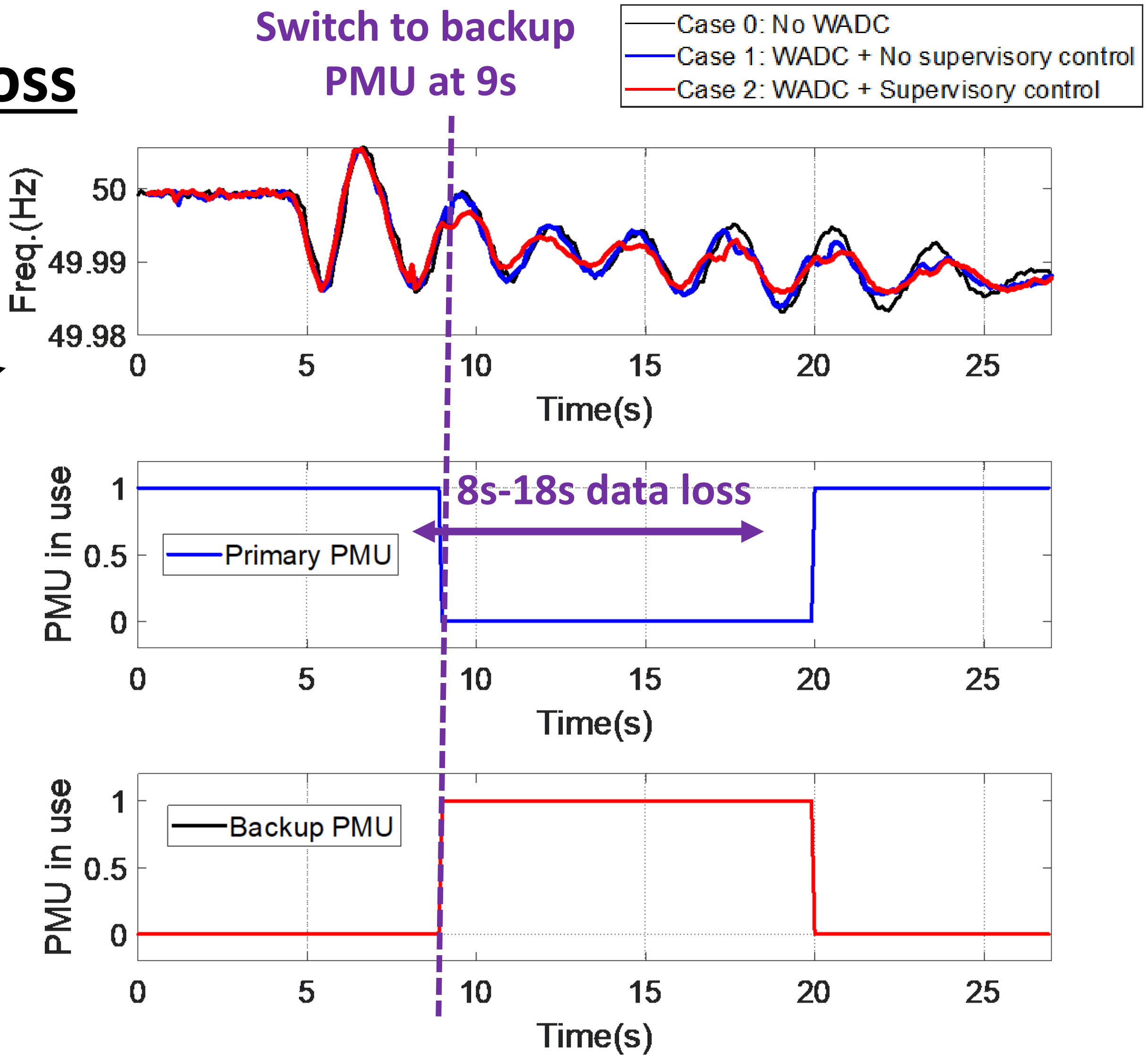
HIL Test Results: Continental Europe Power Grid

- **10-second (8s-18s) consecutive data loss**
  - Case 0: No WADC
  - Case 1: WADC + No supervisory control
  - Case 2: WADC + Supervisory control



Bus frequency in south Italy



Zoom in: 0 to 27s

Summary and Future Work

- Latency and data drop can significantly impact the synchrophasor-based applications, especially real-time feedback control.
- Delay compensator, missing data handling, and supervisory control, etc., are implemented to eliminate these impacts.
- Hardware-in-the-loop test with two realistic power grid model demonstrate that the implemented function modules can guarantee control effect under constant/random time delay and occasional/consecutive data drop.
- Future work
  - Compare controller performance under TCP/IP and UDP/IP
  - Investigate other data quality issues, e.g., bad timestamp

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