Overcoming Standard Limitations in Synchrophasor Systems

PJM PDC Testing Experience

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Outline

• PJM Control Center PDC
• PJM PDC testing objectives
• PDC testing setup
• Tests performed
• Key findings from the testing
• Standard limitations and possible mitigation solutions
• Conclusions
PJM SynchroPhasor Architecture

ISO/RTOs to/from PJM

TOs to PJM

TO Viz from PJM

PJM Internal Network

This diagram provides a high level overview of the SynchroPhasor architecture. PJM’s infrastructure components are redundant.

Steps necessary for prepare for Pen Test:
1. Implement firewall rules to enable Pen Test access
2. Configure ISG to point to production
3. Create Pen Test user accounts with individual TO views

Database with Phasor data and user elections to be processed by fat client

TCP 51433 (SQL Server)

TCP 80 (http)
TCP 808 (Net.TCP)

Load Balancer

TCP 443 (https) TCP 808 (Net.TCP)

Firewall rules to allow IPs of authorized TOs

Decrypt HTTPS

Host Web services to send data to fat client running at TOs
Functional requirements

• Total number of PMUs
  – Data from TOs
    • Installing 300+ PMUs at 100+ substations
    • Building support for 150+ substations
  – Data exchange plan – PMU data from neighboring ISOs
    • MISO: 263 PMUs
    • NYISO: 48 substations with PMUs
  – Total over 500 PMUs and at least to support twice that in near future

• Data forwarded to
  – RTDMS – must be in single stream
  – PI database – must be in single stream?
Objectives

• Determine if PDC will be able to meet PJM synchrophasor system requirements
  – Current needs
    • Getting data from all TOs
    • Adding time-tag to received data
    • Data quality
  – Future needs
    • Sufficient capacity
    • Adequate performance
• Have a clear understanding how PDC works
  – Setting status flags
  – Output behavior under various input conditions
Test setup

- Synchrophasor system simulator
  - Generate various test data streams based on the test case specification
- PMU Connection Tester
  - Capture PDC output data for analysis
Tested scenarios

• Normal condition
• Missing data packets
• Late data arrival
• Flagged PMU data
  – Invalid/PMU error
  – Lost sync indication
  – Sort by arrival
  – Trigger flags
• PMU configuration changes
• PMU data frame CRC error
• Time of Arrival check
• Capacity test
We need PDC standard!

- Size limitation of the standard
  - Could be a major issue
- Standardized way for PDCs to respond to
  - Setting flags
    - Data quality marking
    - Processed data indication
  - Change management (e.g. Add/remove PMUs from a stream)
  - Long interruptions of all input data
Data element size in data and configuration frames
– total bytes must be < 65536 (frame size)

<table>
<thead>
<tr>
<th>Data element</th>
<th>Data frame</th>
<th>CFG-1/2 frame</th>
<th>CFG-3 frame</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Integer</td>
<td>Floating</td>
<td></td>
</tr>
<tr>
<td>Phasor</td>
<td>4</td>
<td>8</td>
<td>20</td>
</tr>
<tr>
<td>Analog</td>
<td>2</td>
<td>4</td>
<td>20</td>
</tr>
<tr>
<td>Digital</td>
<td>2</td>
<td>N/A</td>
<td>260</td>
</tr>
<tr>
<td>Frequency</td>
<td>2</td>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>df/dt</td>
<td>2</td>
<td>4</td>
<td>0</td>
</tr>
</tbody>
</table>
### Ultimate limit – One data element per PMU only

<table>
<thead>
<tr>
<th>Data element</th>
<th>Max. # of PMUs in a data frame</th>
<th>Max. # of PMUs in a CFG-1/2 frame</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Integer</td>
<td>Floating</td>
</tr>
<tr>
<td>One phasor only</td>
<td>10,913</td>
<td>6,547</td>
</tr>
<tr>
<td>One analog only</td>
<td>16,369</td>
<td>10,913</td>
</tr>
<tr>
<td>One digital only</td>
<td>16,369</td>
<td>225</td>
</tr>
</tbody>
</table>
A sample PMU

- One voltage phasor, two current phasors, two analog values, and zero to three digital WORD

<table>
<thead>
<tr>
<th># of Digital WORD</th>
<th>Max. # of example PMUs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>In a data frame</td>
</tr>
<tr>
<td></td>
<td>Integer</td>
</tr>
<tr>
<td>0</td>
<td>3,637</td>
</tr>
<tr>
<td>1</td>
<td>3,273</td>
</tr>
<tr>
<td>2</td>
<td>2,980</td>
</tr>
<tr>
<td>3</td>
<td>2,728</td>
</tr>
</tbody>
</table>
There are several options

- **Limit data element**
  - No digital, positive sequence phasors only
  - May not meet applications requirement

- **Use CFG-3**
  - Can get some relief
  - May not be a long term solution

- **Multiple streams**
  - Can be a solution
  - Complication on receiving side

- **New standard or standard revision**
  - Preferred but will take some time
• PDC testing is important to
  – Understand how they function
  – Whether they can meet system functional and performance requirements, and
  – Whether they are interoperable with other system components
• Using synchrophasor system simulator is an effective way to perform such tests
• For large-scale synchrophasor systems, current standard will become a major limitation in transporting synchrophasor data
  – Configuration frame CFG-1/CFG-2 is the bottleneck
• There are some mitigation options
  – Standardized approach is preferred
Questions?