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Quantifying Control Loop Stability Measures and ICT Network Latency Requirements in Wide-Area Control Design

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PART I

Signal Observability - Control loop stability – Delay Margin

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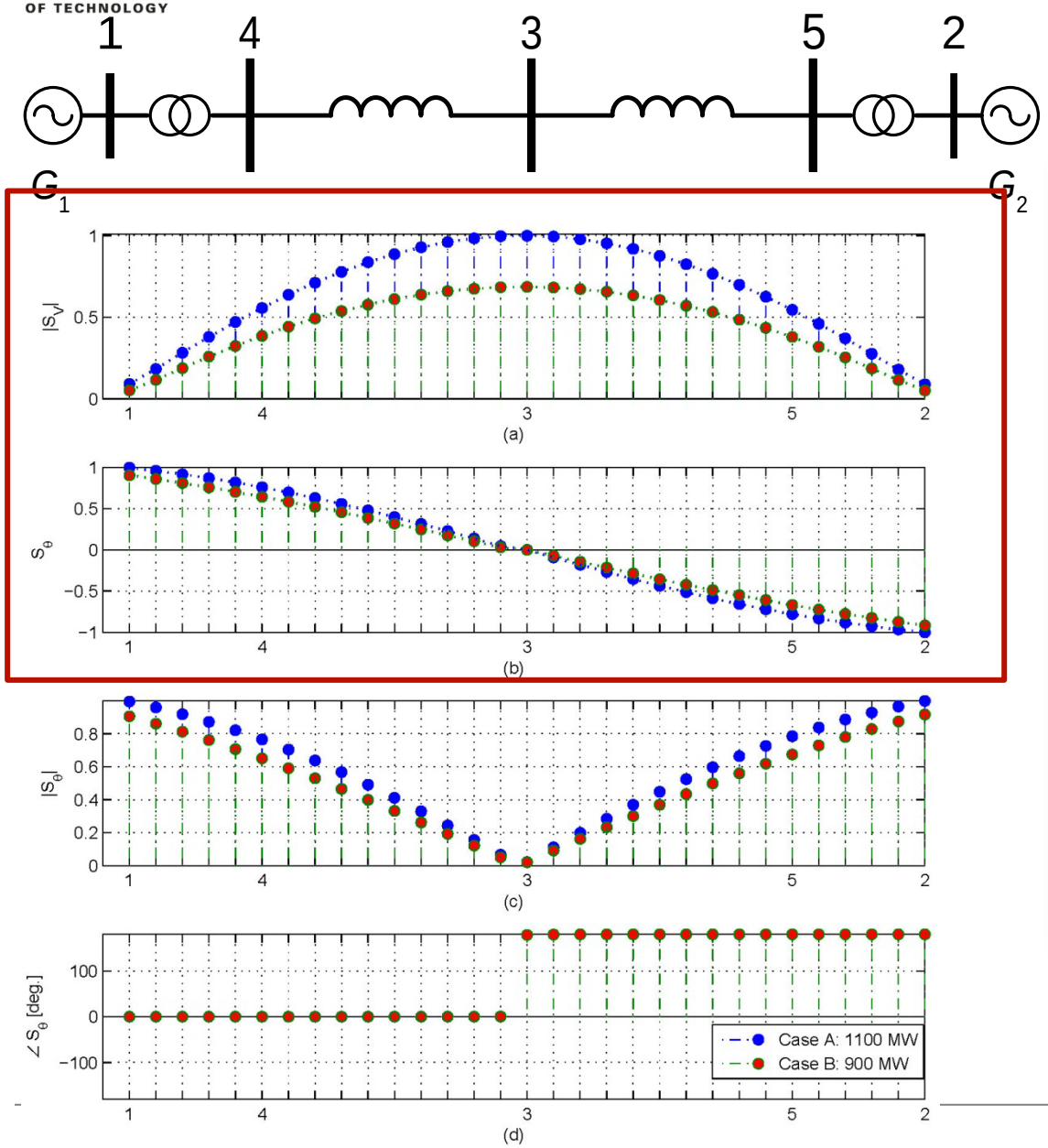
Part I

- Dominant Path Concept– Network Modeshape: a brief summary
- Feedback properties of dominant path signals:
  - Relationship between network modeshape and delay margin
- Impacts of time delays on frequency and time responses

Signal Observability: *Dominant Path Concept*

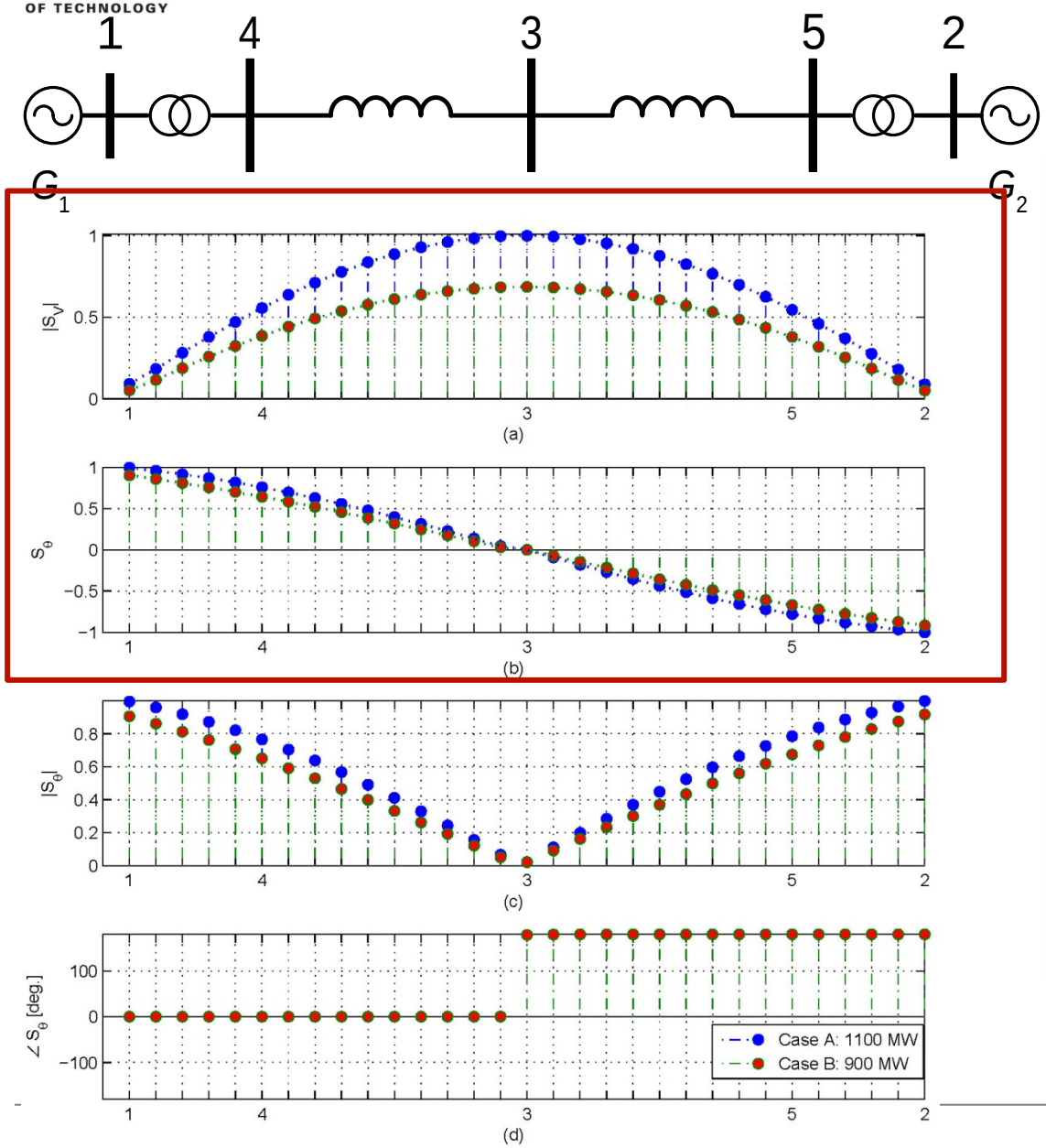


Network Modeshape

- the product of electromechanical modeshape and network sensitivities

- Voltage Magnitude Modeshape: S_v
- Voltage Angle Modeshape: S_θ

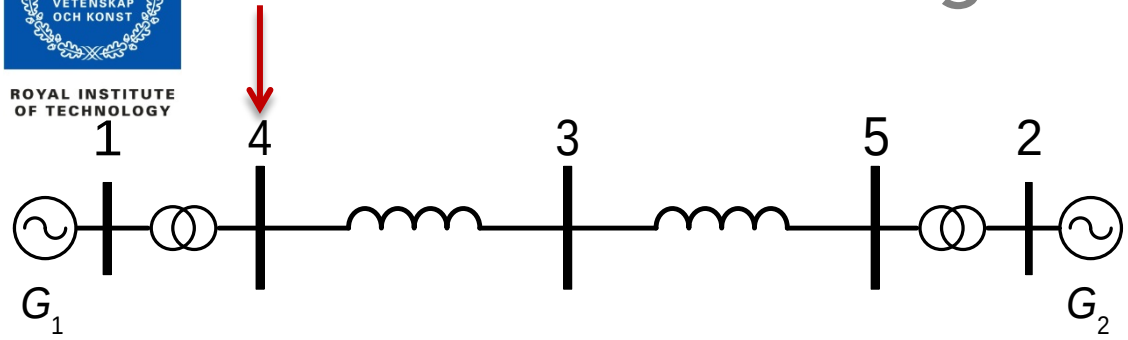
Signal Observability: *Dominant Path Concept*



Important Features

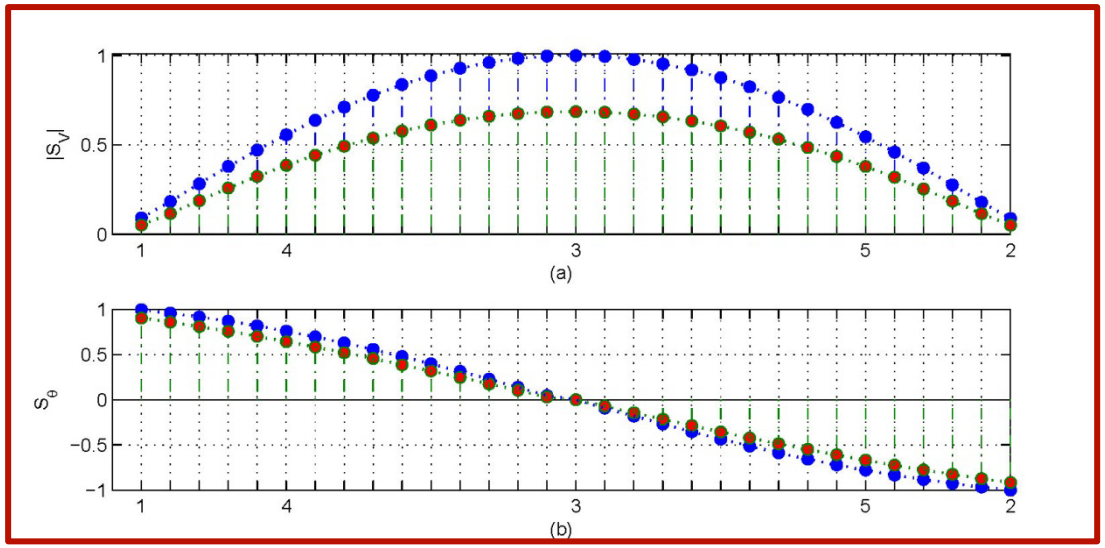
- ✓The largest S_V or the smallest $|S_\theta|$ element(s) indicates the center of the path.
- ✓The difference between S_θ elements of two edges of the path is largest among any other pair within the same path.
- ✓S_V elements of the edges are the smallest or one of the smallest within the path.
- ✓The inter-area contents of S_V are more observable in a highly stressed system.

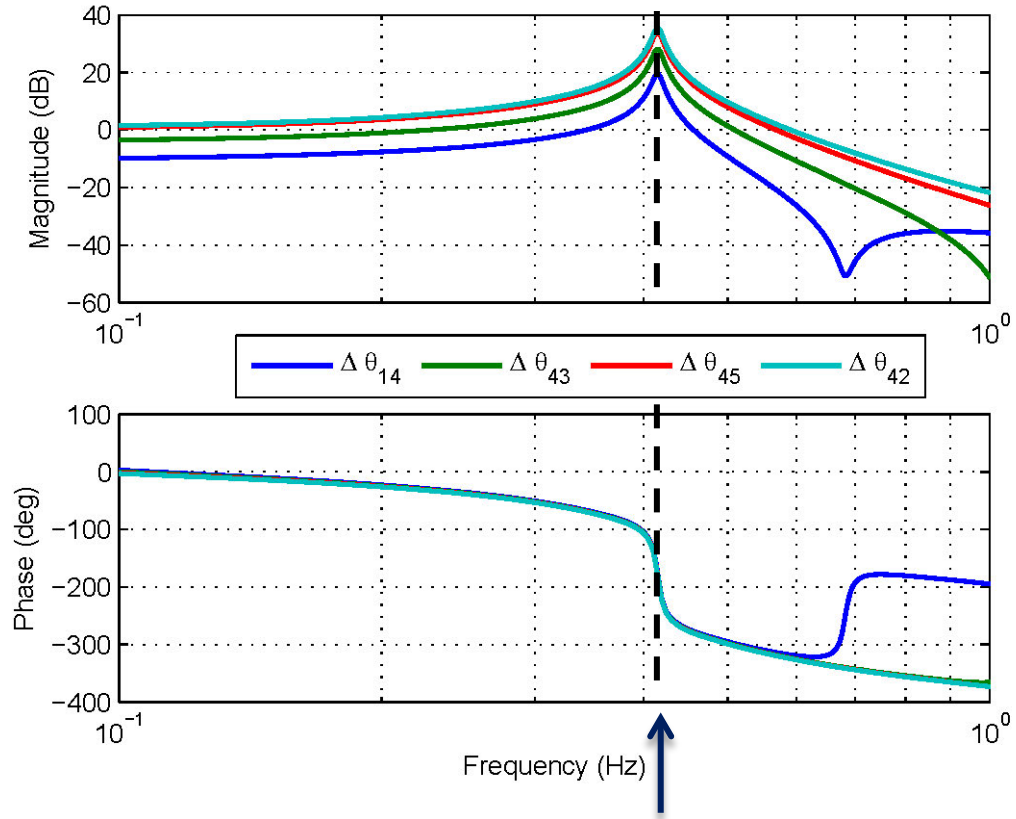
Dominant Path Signals: Frequency Responses



Voltage Angle Difference $|\theta ij|$

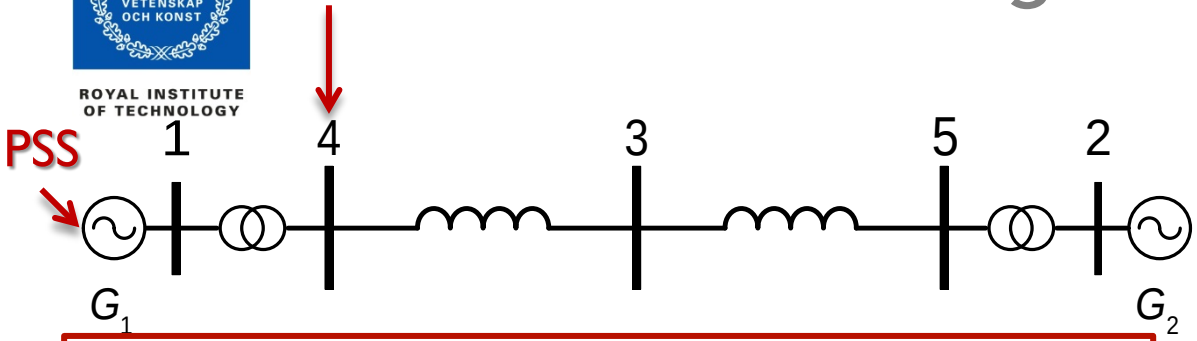
Bode Plot





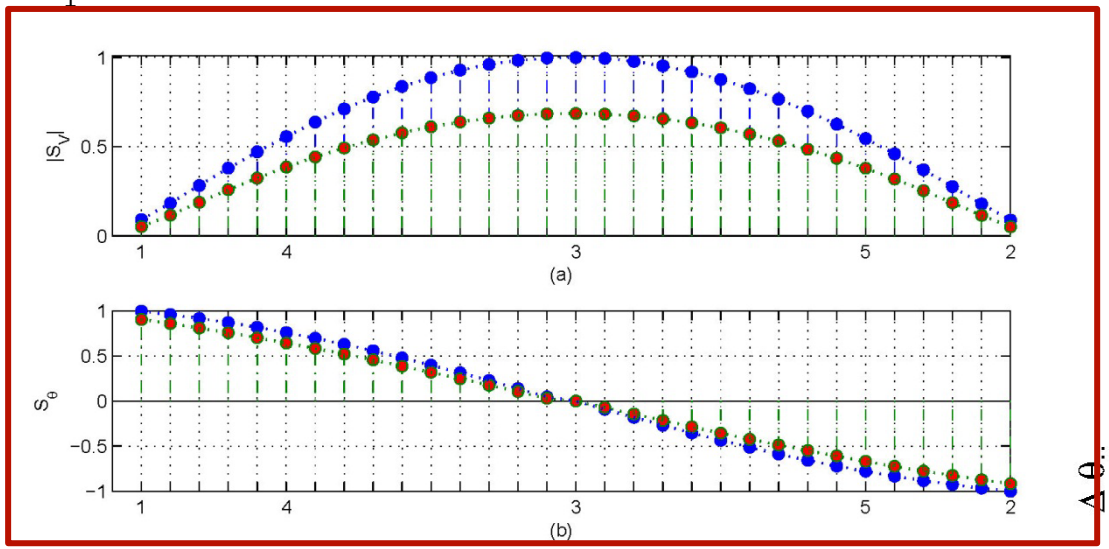
Inter-area frequency

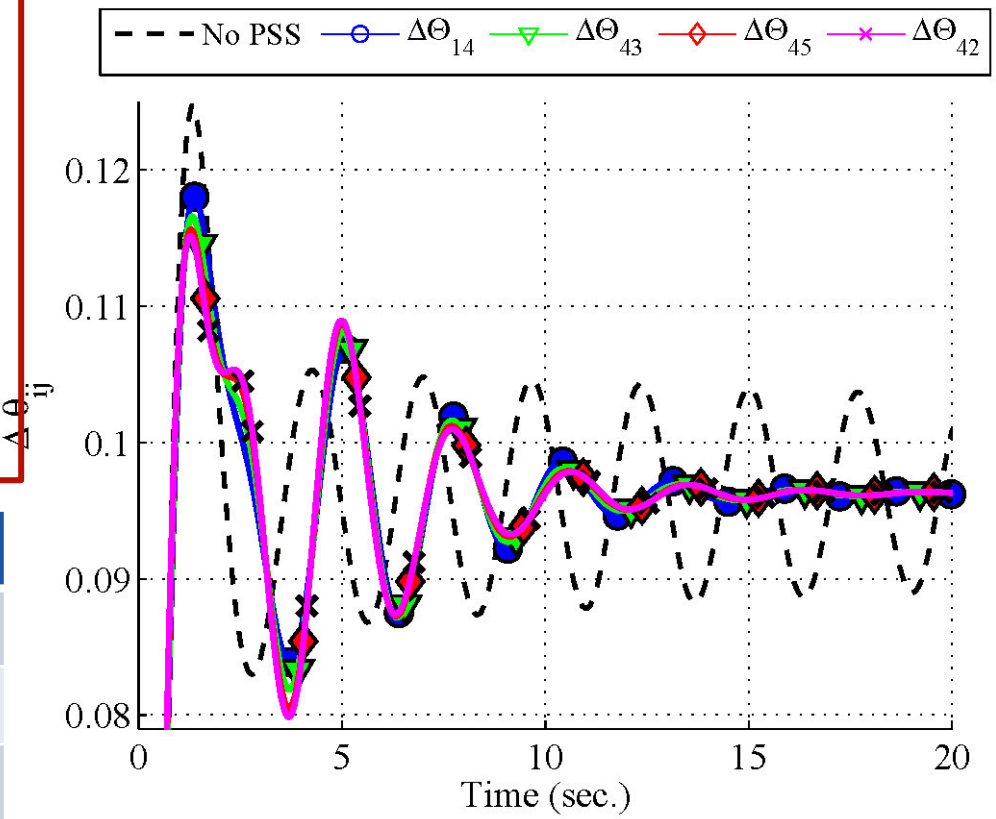
Dominant Path Signals: Damping Performance



Voltage Angle Difference | θij|

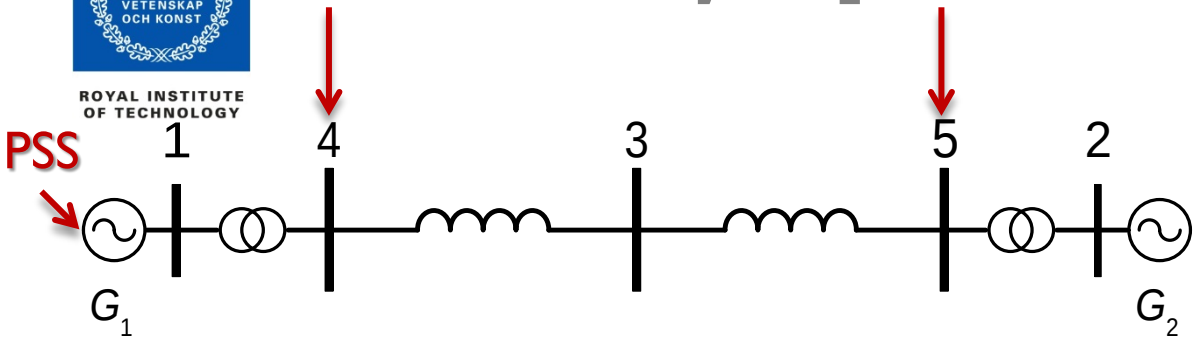
$\zeta = 15\%$



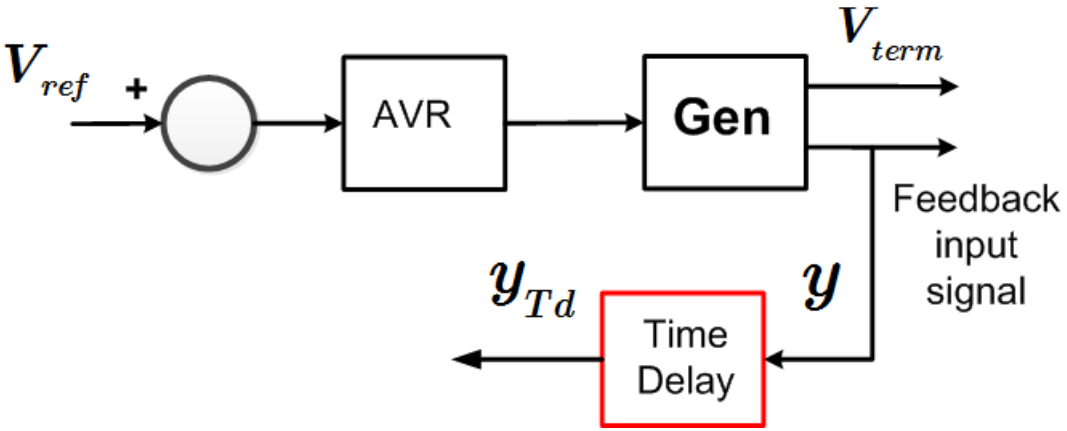


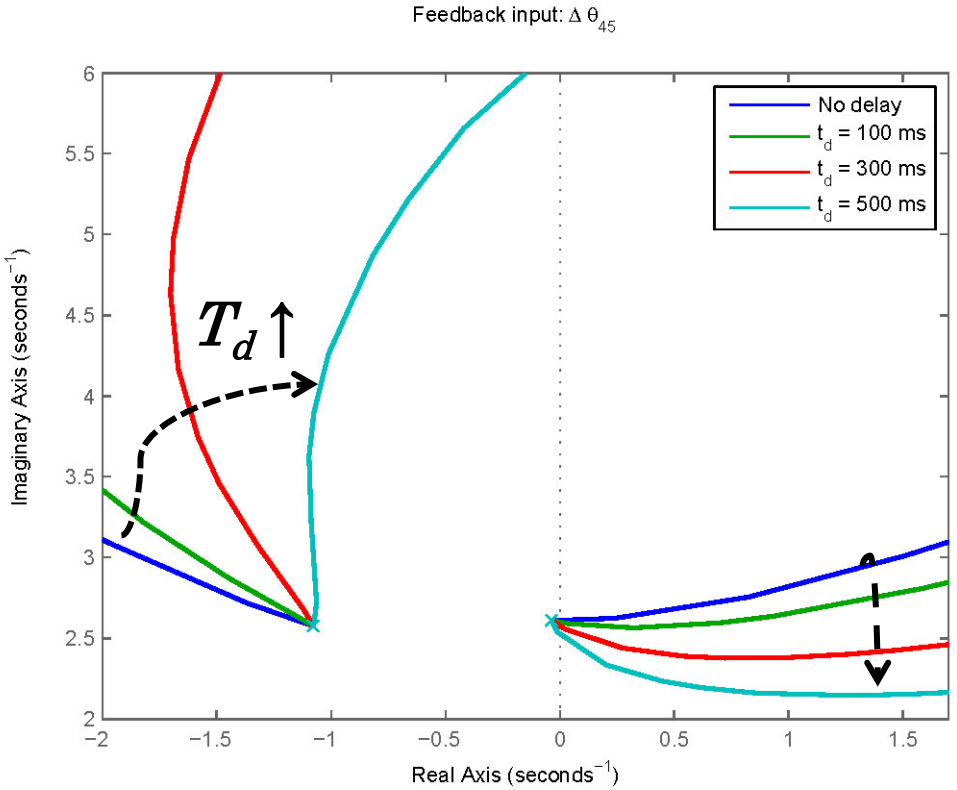
Signals	PSS Gain	Mp(%)
$\Delta\theta_{14}$	130.51	18.02
$\Delta\theta_{43}$	55.87	16.58
$\Delta\theta_{45}$	34.85	15.61
$\Delta\theta_{42}$	33.47	15.14

Time Delay Impacts: OL Frequency Responses

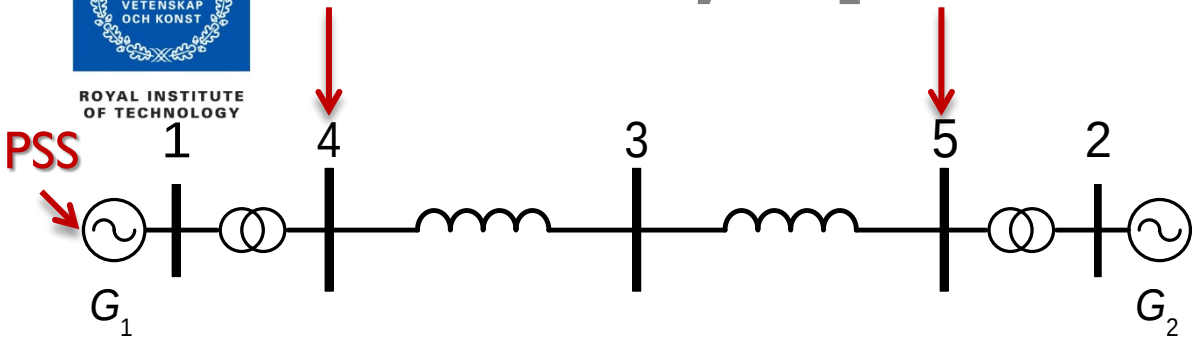


Root Loci: $\Delta\theta 45$

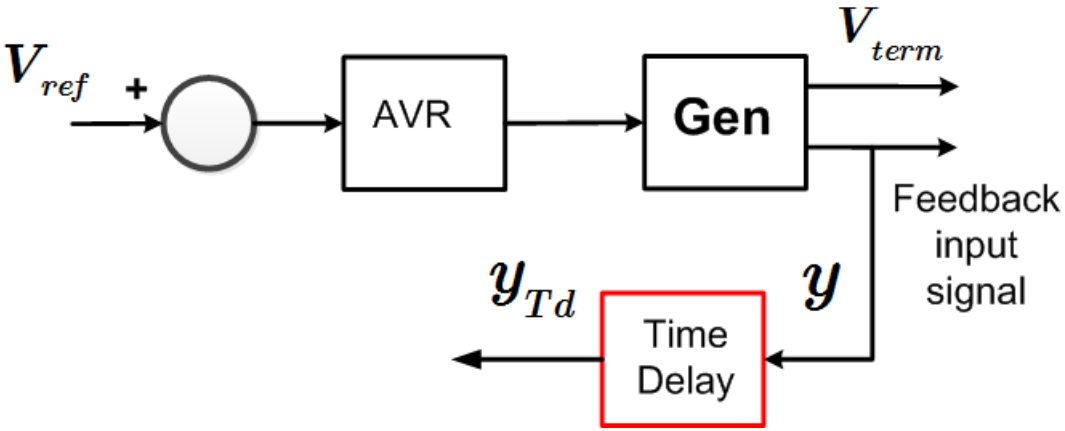


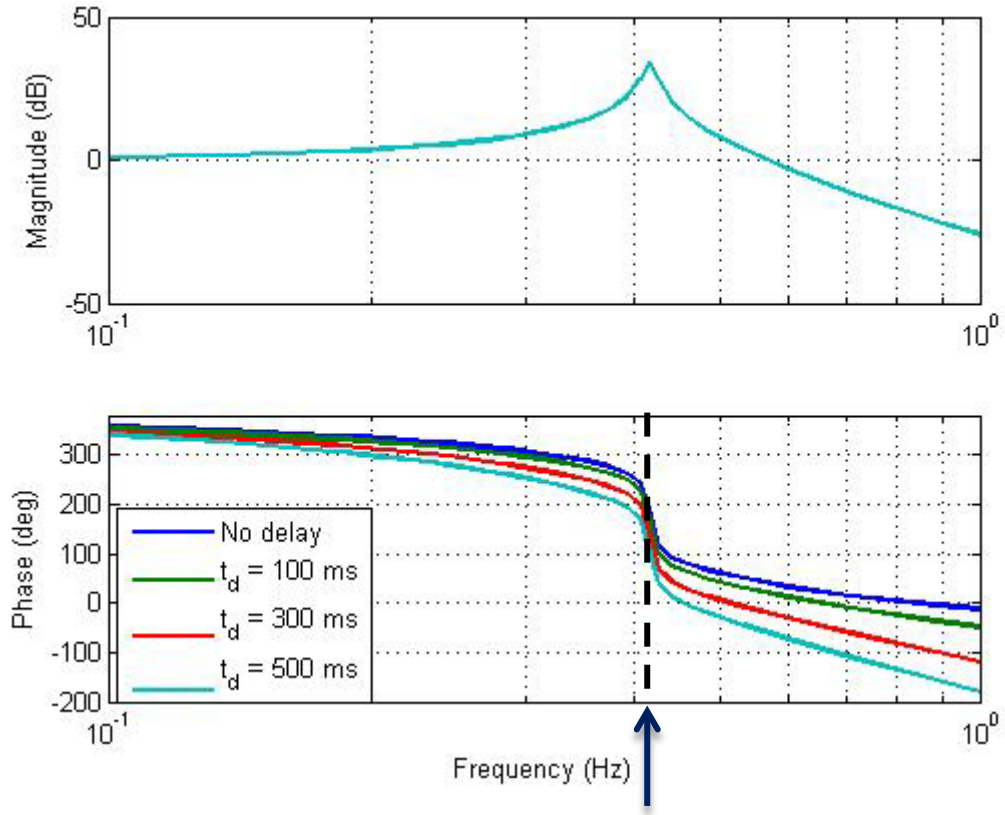


Time Delay Impacts: OL Frequency Responses



Bode Plot: $\Delta\theta 45$

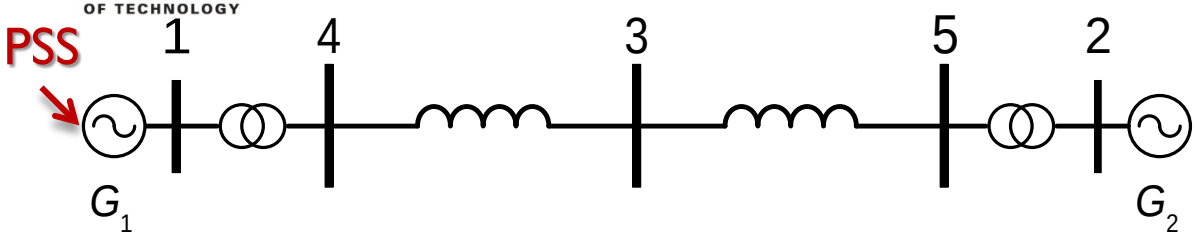




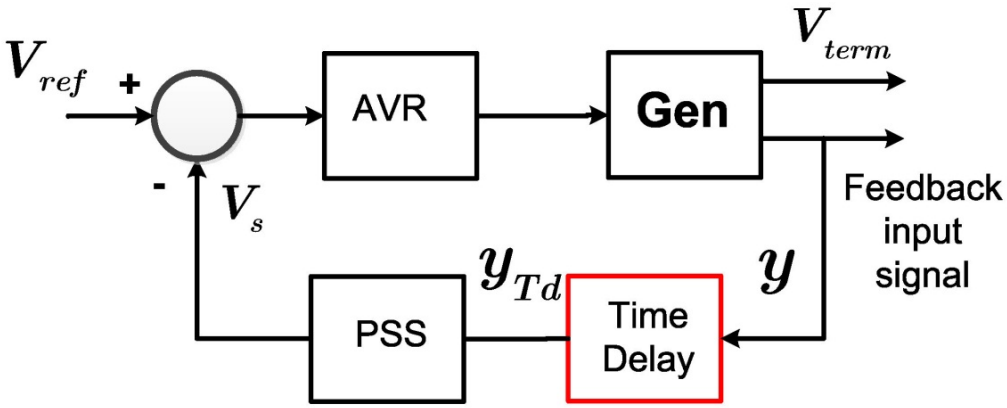
Time delay ≈ phase lag

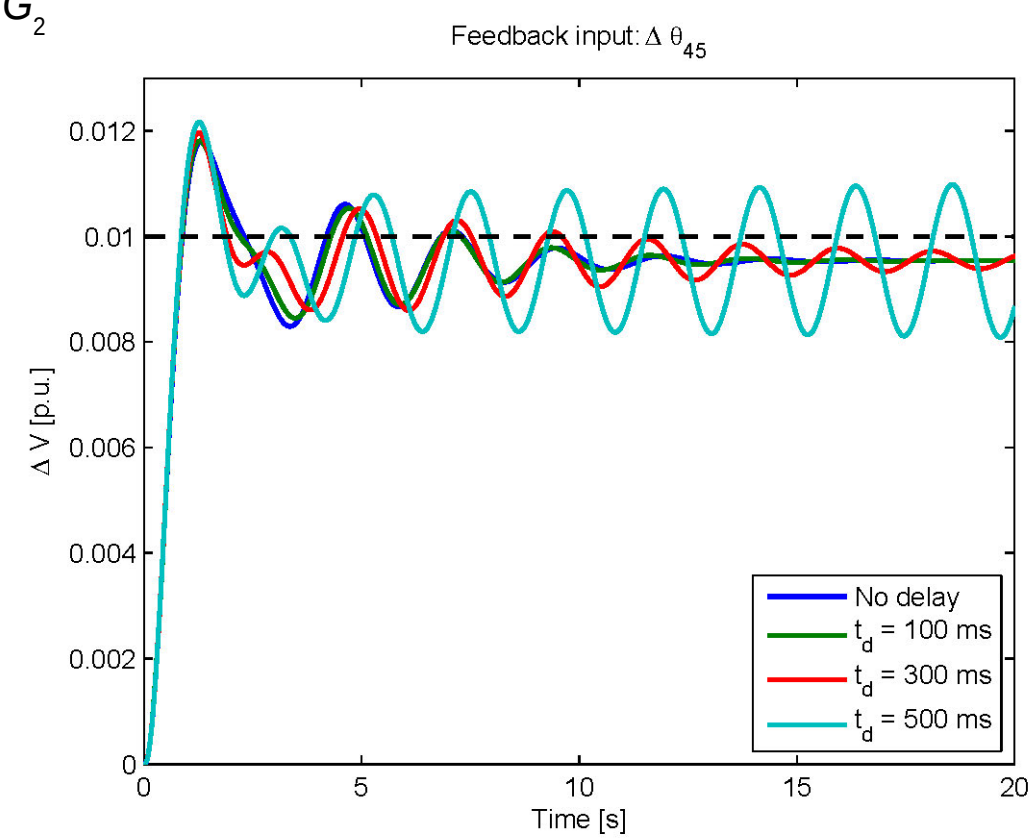
Inter-area frequency

Time Delay Impacts: CL Time Responses



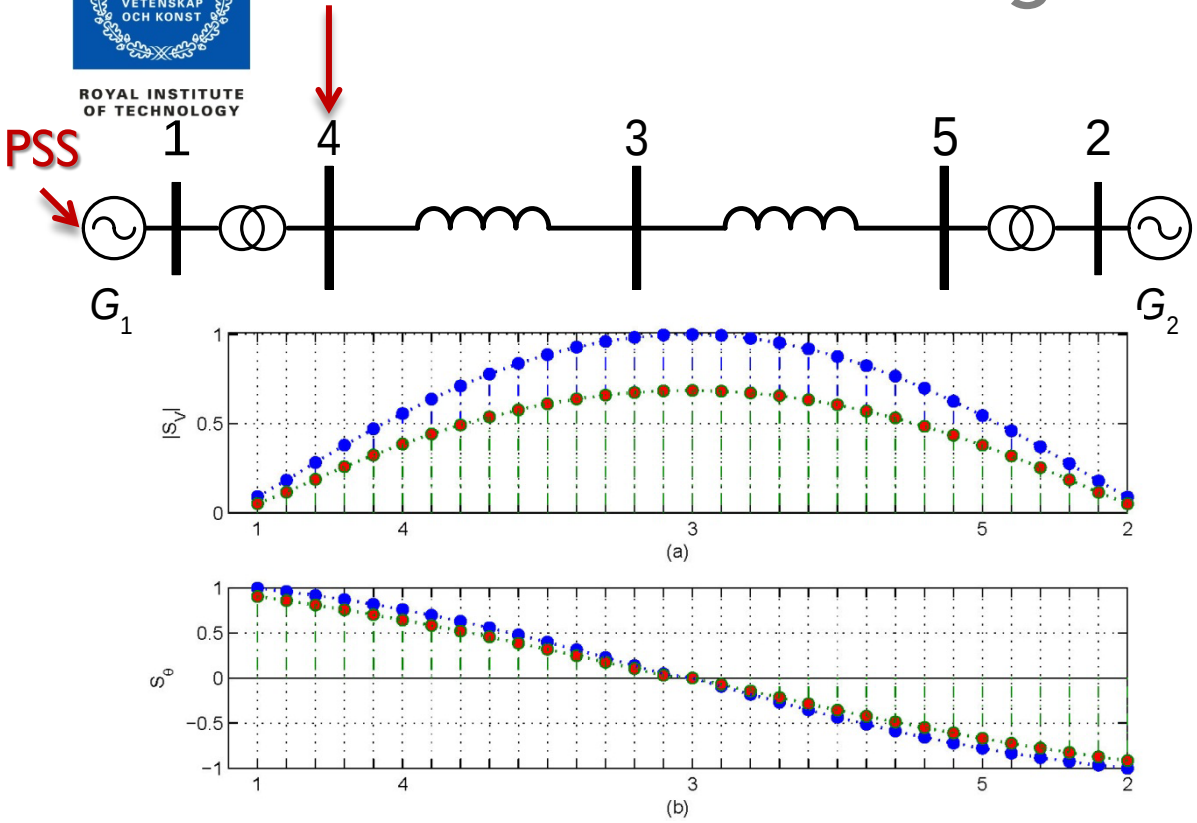
$\Delta\theta_{45}$



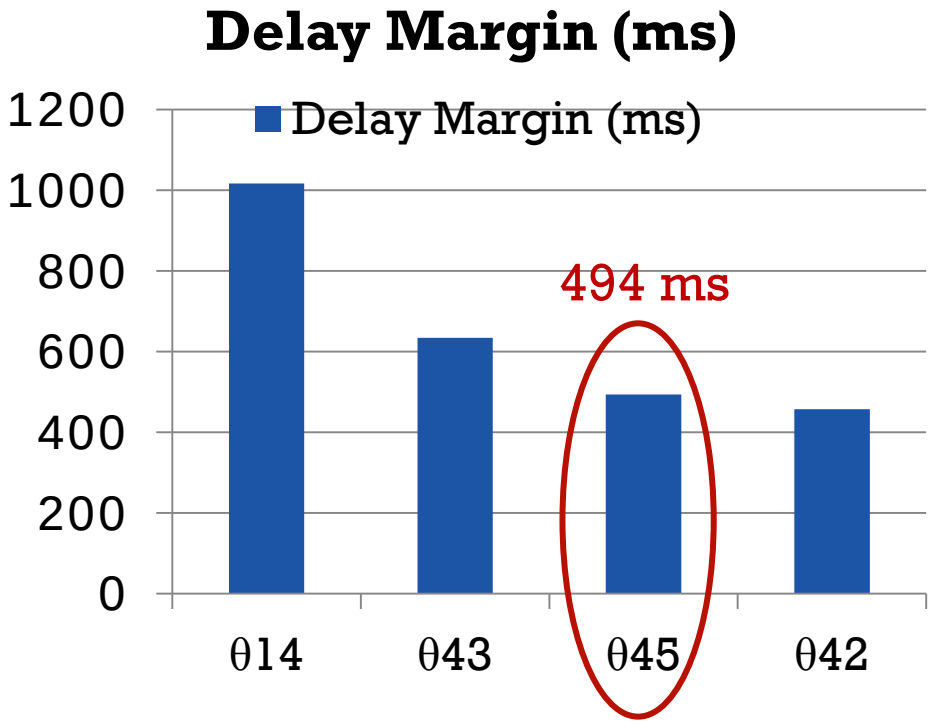


Time delay ≈ phase lag

Dominant Path Signals: Delay Margin



Voltage Angle Difference | θij|



- Delay margin = upper bound for the design of WAPOD

- Althought it's attractive to use the signals with the largest observability, we found that these signals result in a smaller delay margin.

Delay Margin (DM) is defined as the smallest time (for Td > 0) required to destabilize the closed-loop system.

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PART II

Equivalent Time Delay (ETD) – ICT delay requirements

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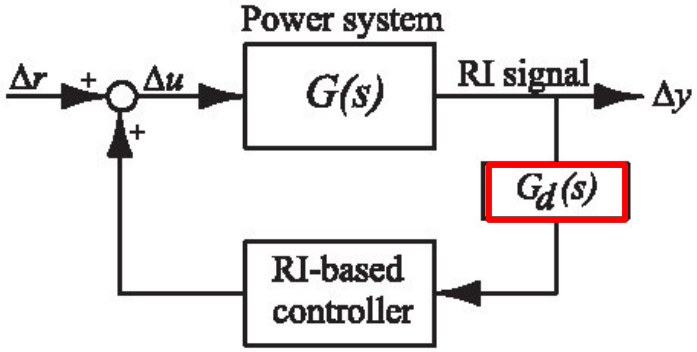
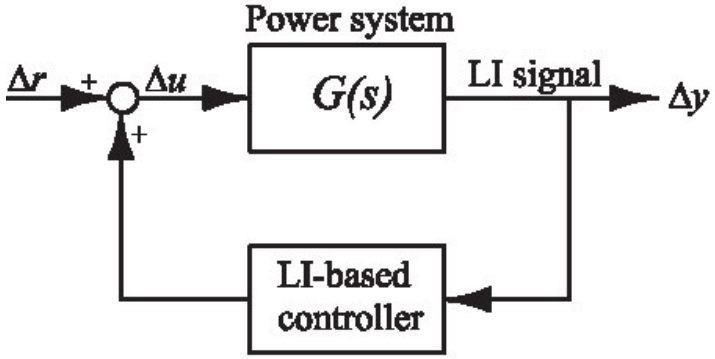
Part II

- Equivalent Time Delay (ETD): Definitions & Usages
- ICT Delay Requirements
- Methodology Demonstration (on both small and large systems)

How to assess a controller's damping performance using LI and RI Signals?

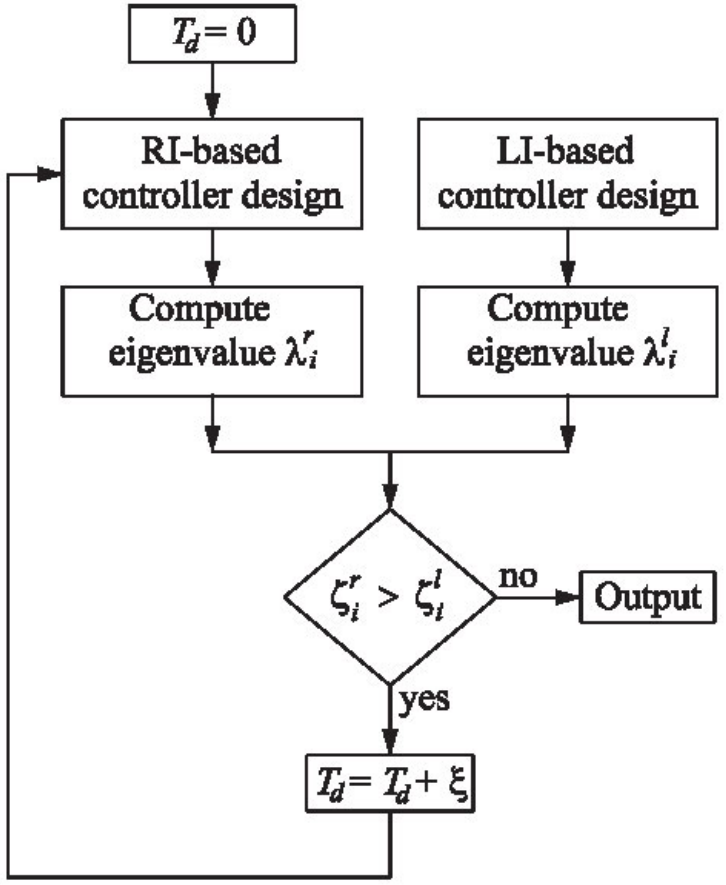


RI-based controller



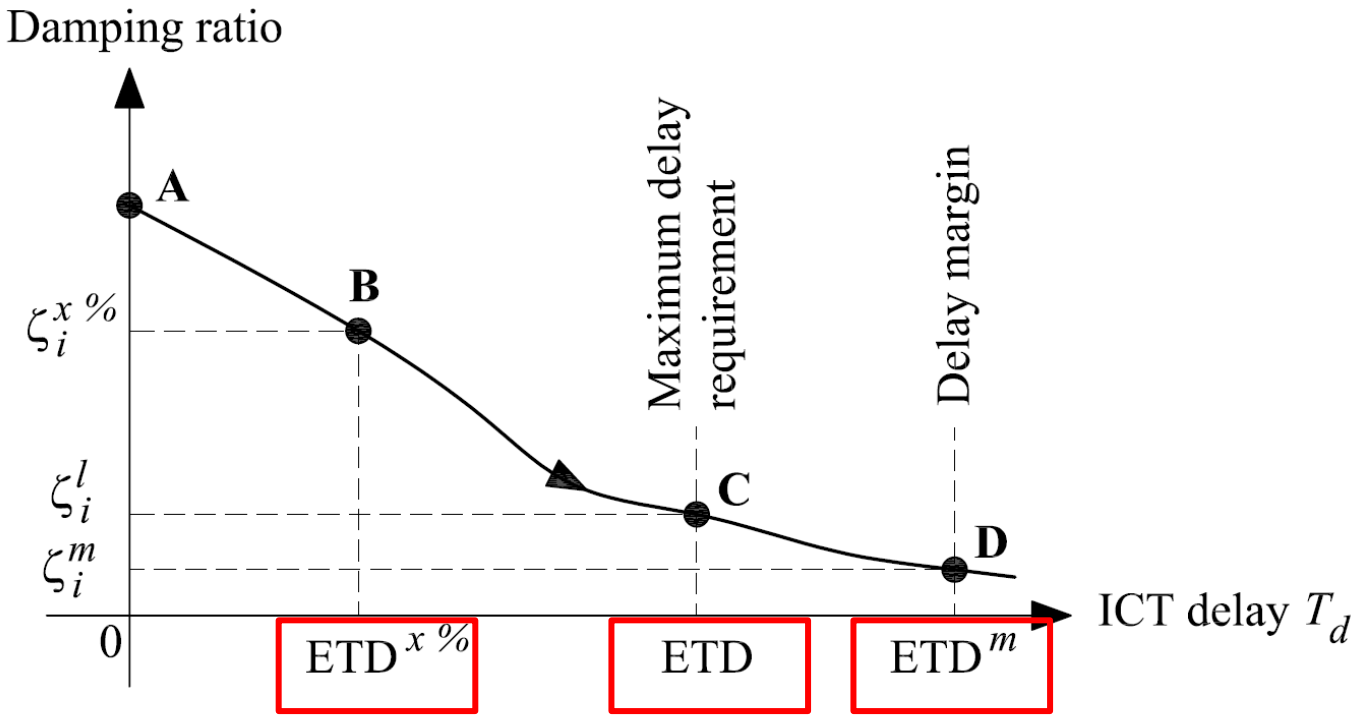
LI-based controller

ETD Calculation Method



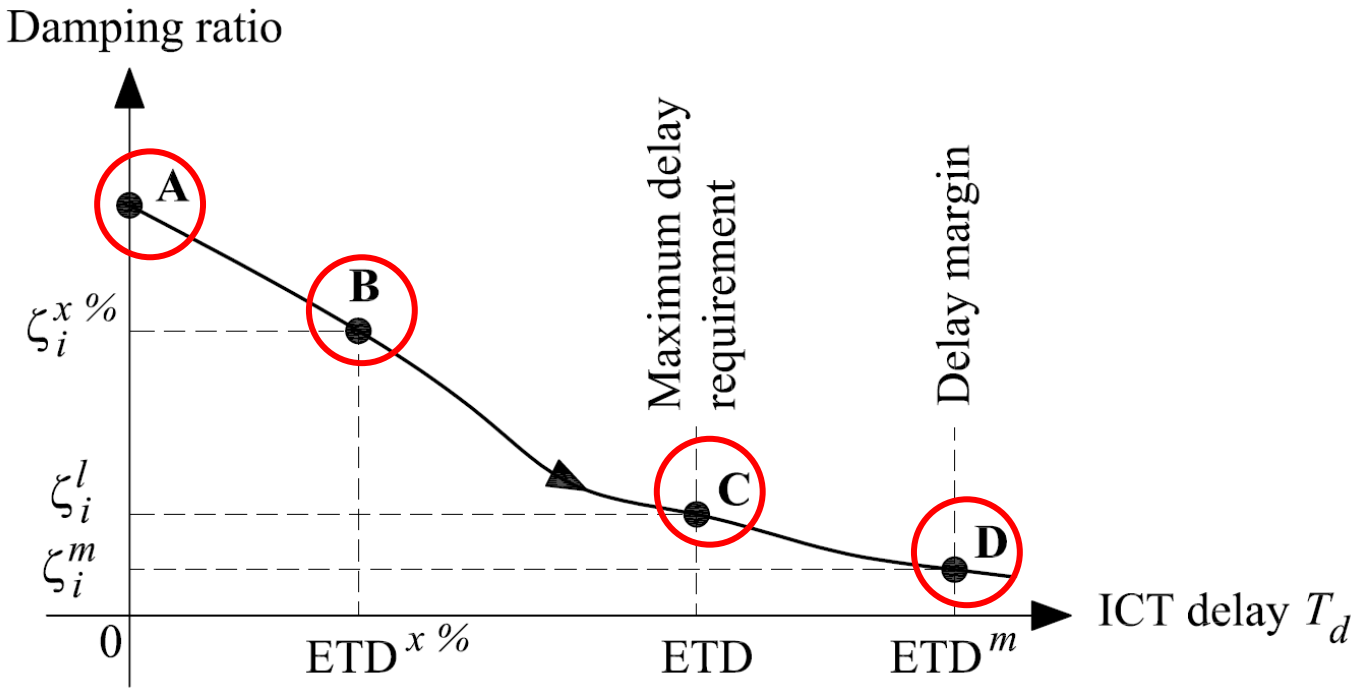
- **ETD** is a time value for which **Remote Input (RI)-based controller** presents the **same damping** as **Local Input (LI)-based controller**

Equivalent Time Delay (ETD) (1/2)



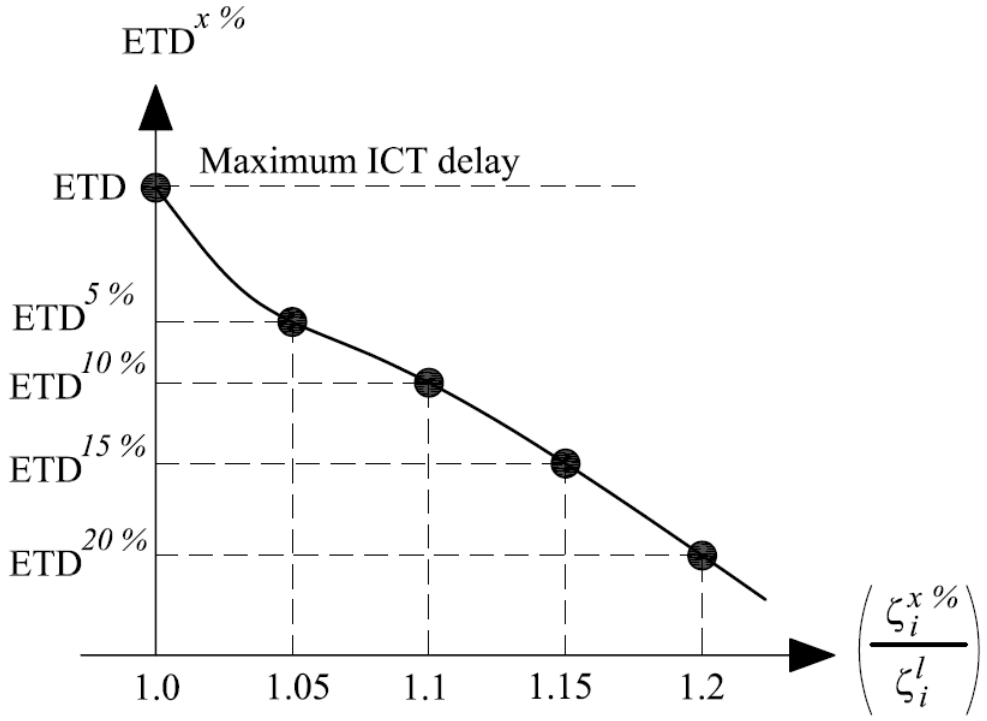
- **ETD$^{x\%}$** : allowable time delay at which the RI signals have a damping ratio which is x% higher than when using the LI signals
- **ETD** presents the **maximum time delay** of a wide-area measurement to provide *the same damping* as a LI signal
- **ETD^{m}** : allowable time delay up to the stability margin, i.e. delay margin

Equivalent Time Delay (ETD) (2/2)



- A: Maximum damping level at zero delay
- B: $\zeta_i^{x\%}$ is defined as the improved damping required to provide x% of damping enhancement compared to the local signal
- C: where RI-based controller yields the same damping as LI-based controller
- D: delay margin ETD^{m} (maximum allowable delay)

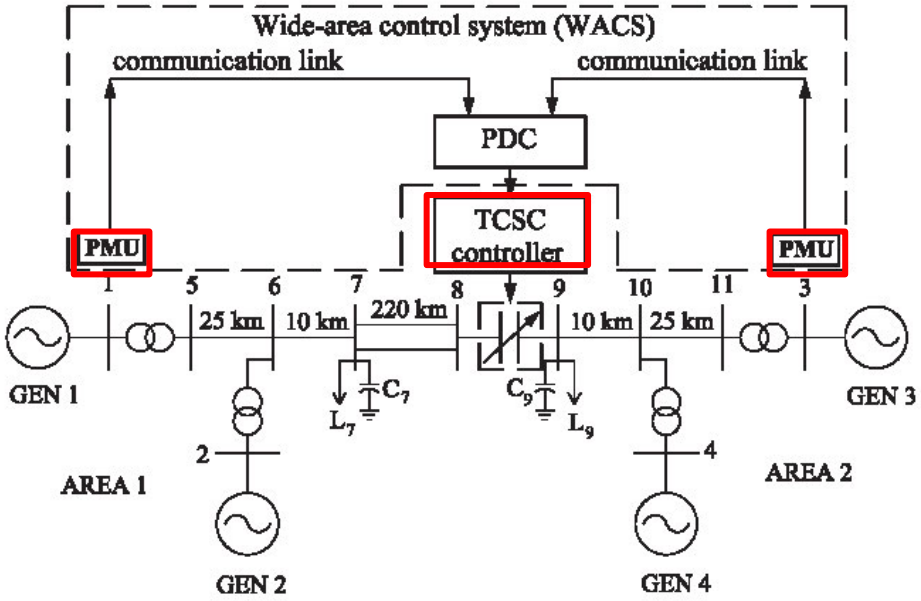
ICT Delay Requirement



- WACS must provide a delay allowing the controller to attain a certain damping improvement over the controller using local signal.
- Allowed ICT delay requirement can be considered as a design standard for WACS.

Methodology Demonstration: TCSC Design

Test System 1

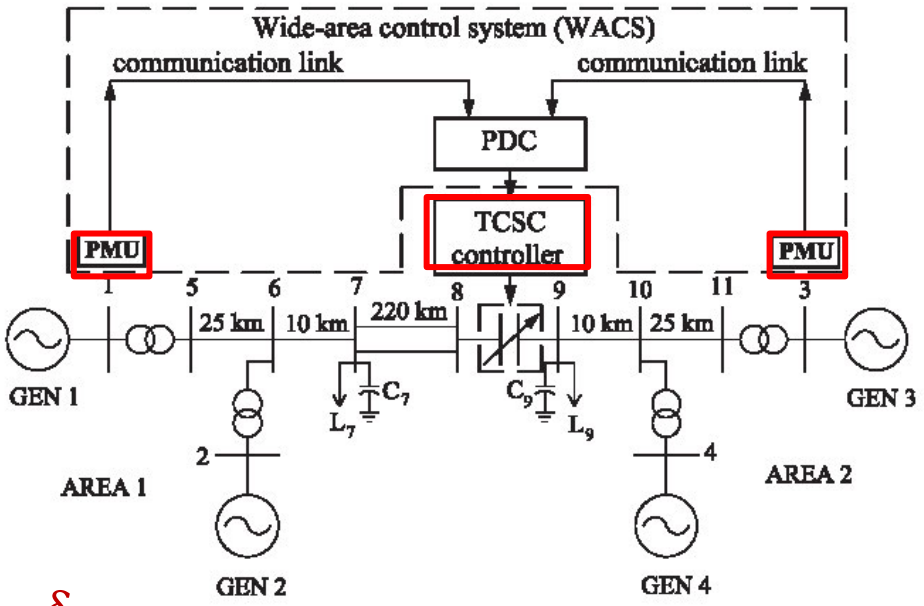


	Inter-Area Modes	Frequency (Hz)	Damping (%)
Without TCSC	$-0.104 \pm j3.367$	0.54	3.10
RI-based TCSC	$-0.615 \pm j3.586$	0.57	16.9
LI-based TCSC	$-0.388 \pm j3.449$	0.55	11.2
ETD	194 ms		

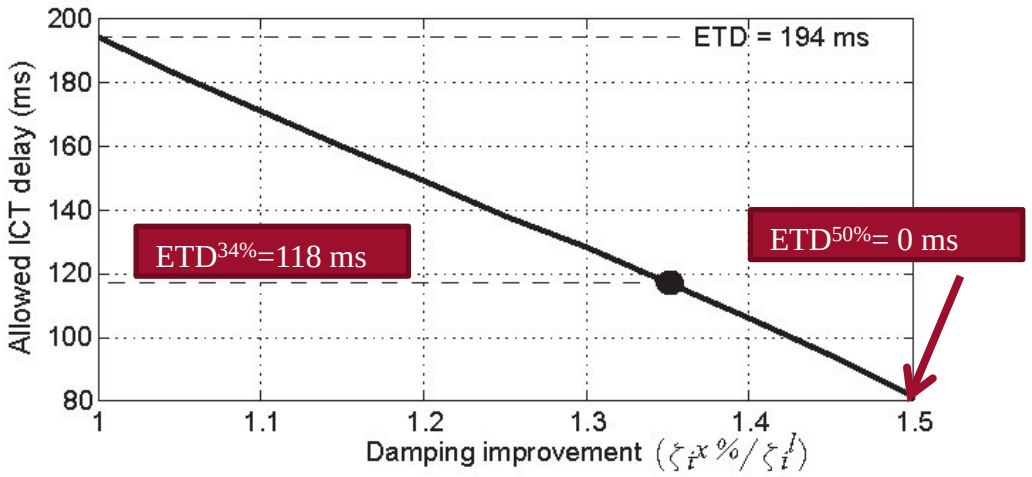
Td is assumed to be zero!

Methodology Demonstration: TCSC Design

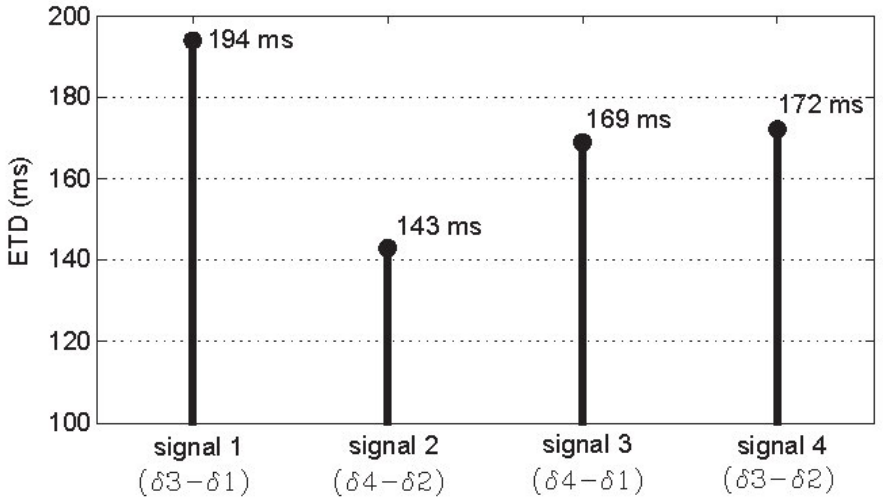
Test System 1



Input Signal: $\delta_3 - \delta_1$



ICT delays required for damping improvement

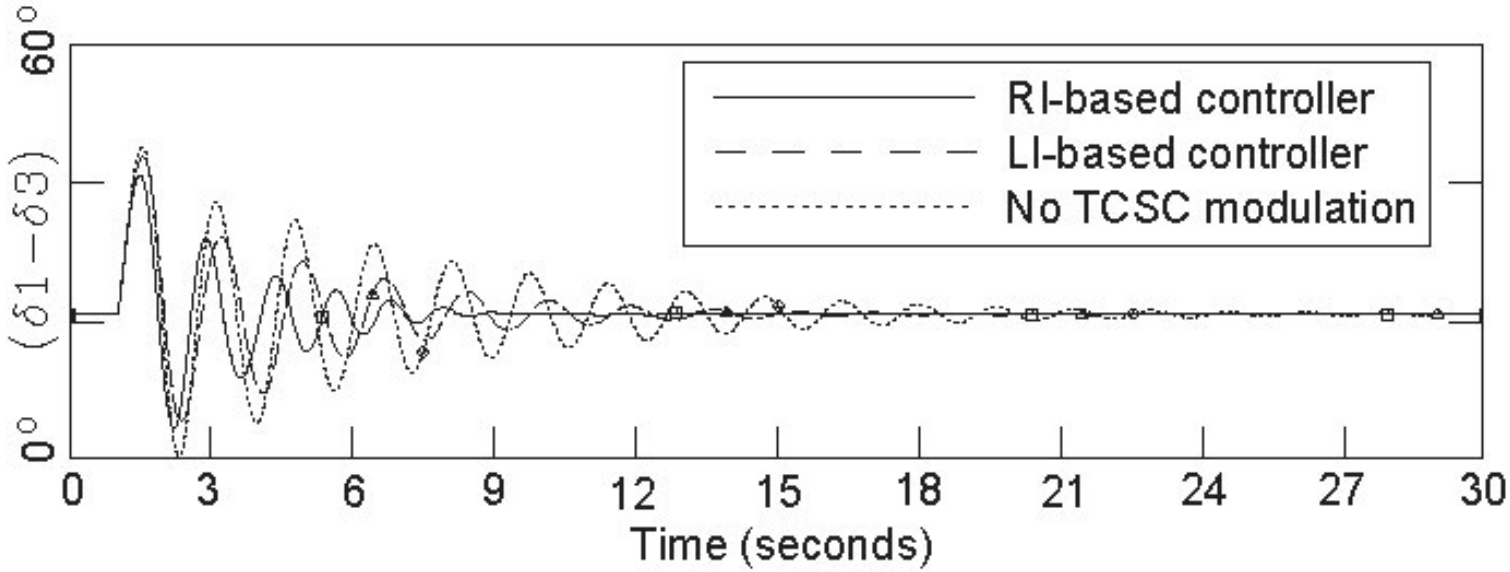


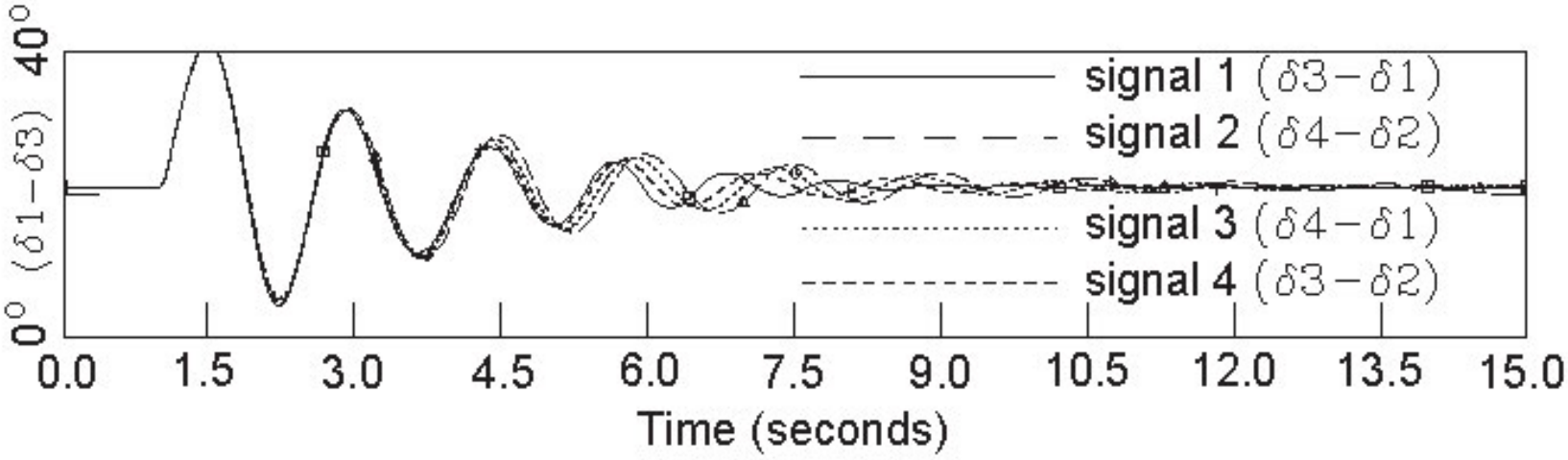
ETDs for different wide-area signals

Methodology Demonstration: TCSC Design

Validation through non-linear simulation: 3-ϕ fault for 100 ms

Td = 118 ms





Comparison among different remote signals

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Conclusions

- Network modeshapes of the dominant path signals provide a measure to select signals having high observability of any mode of interest.
- ICT delay requirements for WACS are defined by ETD.
- Delay margin poses the upper bound for the design of WAPOD while ETD provides the lower bound (which the wide-area controller performs equally as the local-based controller).
- Thus, it is only beneficial to employ wide-area signals when the ICT delays are less than the ETD.
- Capital and operational expenditure costs of the ICT network have to be considered in practice.
- Laboraty tests for validation of the proposed methodology are needed.

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Thank you!

Questions?

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