

# **Data Validation &** Conditioning





**Electric Power Group** 

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### Presentation

- Introduction of project
- Task 1 survey
- Task 2 recommendations
- Task 3 algorithm
- Algorithm description





## Introduction

- Data Validation and Conditioning Project
  - Awarded to EPG in December 2012
  - Completion by October 2014
- Three stages
  - Stage 1 survey, study, & prototype development
  - Stage 2 prototype demonstration
  - Stage 3 prototype functional specifications



## **Principle objective**

- Develop, test and prototype various methods for conditioning and validating real-time synchrophasor data
  - Applicable to SGIG projects
  - Usable in deployed architectures
  - Include consideration of design & deployment
- Output includes cleaned data & quality flags



### **EPG Proposal**

- Issues go deeper than data
  - Equipment selection & compatibility
  - System design
  - System administration
  - Operation and maintenance
- Ties all aspects together
- Data validation
  - Real-time
  - Data itself





### **EPG Proposal and Plan**





#### Phase 1, Task 1 Review Existing SGIG Systems

- Surveyed 20 companies that have SGIG projects or significant synchrophasor development
- Reviewed literature-sources NASPI, IEEE, etc.
   Findings:
- System Administration tailored to project
- Various design procedures generally seemed adequate
- Implementation checkout procedures usually minimal
- Few operational Data Validation Systems
- Most utilities planning future expansion



### Phase 1, Task 2

**Best practices recommendations** 

- Drew up best practice recommendations based on -
  - Survey practices that work
  - EPG experience in working with companies

#### **Best Practice Recommendations**:

- Recommend multi-disciplinary system administration
- Coordinate between parties working on the project
- Validate the system at every level to be sure the measurements are accurate and correctly identified
- Use on-line data validation catch problems
- Institute a maintenance program





### Phase 1, Task 3

**Algorithm development & initial testing** 

#### Algorithm development – approach:

- Create a generic enough algorithm for wide use
- Use existing validation methods as much as possible
  - C37.118 validation flags
  - Additional primary considerations like message format
- Use secondary considerations that are available
  - Communication interface flags
  - Known data relationships & reasonable limits
- Offer methods using system relationships, but not requiring a full model



# **Data Validation and Conditioning** Algorithm



# Algorithm is as series of processes

- Input data converted to FP-polar
  - No loss of resolution
  - Can separate phase (time) and amplitude errors
- Processes follow logical progression
  - After some errors, no further processing needed
- Data output can be with or w/o conditioning
  - Conditioning declares data bad by setting to NaN
  - Data flags can be included



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## Initial – communication, format, & time

- Communication error
  - From the interface, such as frame error, dropped TCP link, etc.
- Message format error
  - Frame too long, bad CRC, wrong PMU-ID
- Time stamp error
  - Time within bounds
  - Message out of sequence
- Latency calculation
  - Within user set bounds
  - Large variation
- These error types also can provide security (intrusion)





## Second – 118 flags & data characteristics

- C37.118 status flags indicate many detectable problems
  - Data validity, time stamp, and modification
  - Time synchronization
  - PMU error
  - Small differences between 2005 & 2011 versions
- Data characteristics
  - Continuing repetition of values (stale or "stuck" output)
  - High noise (signal content above passband)
  - Readings within H/L limits
  - Values that invalidate other measurements (frequency from voltage phasor)





### Last stage – topology & output

- User configurable topology
  - Generic math & logic available  $(+, -, /, *, =, \leq, \geq, \neq, \text{ etc.})$
  - Combine signals to detect possible errors
    - Sum of currents through a bus
    - Match currents at ends of lines
    - Match voltages on connected busses
    - Other appropriate combinations
- Bad data set to NaN to prevent further use
- Data with fatal errors always set to bad (NaN)
- Dual outputs
  - Output partially conditioned with flags (only fatal errors cleaned)
  - Output with fully conditioned data





## **Data Quality Flag**

<ul> <li>Data quality flag – 8 bit</li> </ul>	QQ	SSSS	LL	
<ul> <li>Flag for each value</li> </ul>	lity	atus	imit	
<ul> <li>Phasor magnitude , angle,</li> </ul>	Qua	b-st	Li	
<ul> <li>Frequency &amp; ROCOF</li> </ul>	-	Su		

- Can be sent in 118 stream 2 flags into integer analog/digital
- Quality good, bad, uncertain, reserved
- Sub-status reason for the quality indication
- Limit value at H/L limit, cannot move, or ok
- Flag similar to OPC DA or field-bus flag





### **Project status**

- Phase 1, Tasks 1 & 2 complete
- Phase 1, Task 3 near completion
  - Conceptual development completed
  - Software developed & test ongoing
  - Last 2 reports nearly complete
- Phase 2, Task 1 started concurrently
  - Developing test algorithm











## **DV examination diagram**

 Overall DV flow diagram



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